MCIMX8M-EVK (mScale850 Customer Board) Schematics DevBoard

Table of Content

Page 1	Cover
Page 2	Block Diagram
Page 3	PWR TREE
Page 4	CPU PWR
Page 5	LPDDR4
Page 6	CPU IO
Page 7	CPU PHY
Page 8	CPU MISC
Page 9	eMMC/NAND/TF/QSPI
Page 10	PMIC
Page 11	BOOT CFG
Page 12	USB
Page 13	HDMI
Page 14	CODEC
Page 15	Ethernet
Page 16	WiFi/BT
Page 17	PCIe
Page 18	MIPI/DSI/CSI
Page 19	MicroSD/IR/LED/BTN
Page 20	Debug
Page 21	EXP CN
Page 22	NOTE
Page 23	IOMUX
Page 24	
Page 25	
Page 26	
Page 27	
Page 28	
Page 29	

Revision History

Rev. Code	Date	By		Description
A	2016-12-09	Javen	1	Revision preliminary version
A1	2017-05-26	Javen	1	Change J1401 M.2 connector from sink type to non-sink type
			2	Update U1001 schematic lib
			3	Add R760 to control the VDD_SNVS_0V9 power up sequence
			4	DNP D903, R915, change R936 to 44.2K, Add R942,R943,D910
			5	Change R715 to 10K, add R761 44.2K OHM/0402,C799 1uF/0402
			6	Add Q1402-Q1404, R1458-R1462, C1439-C1441 to prevent current drop during power up due to CAP,DNP C1418,C1419
			7	Add R1802, R1803 to keep VIO voltage for IO REF
			8	J801 change to femal header
			9	Change D1702,D1703 connection to reduce the CP2105 Program step
			10	Change R934 to 1K OHM
			11	Add R845,R846 for backup
			12	Add C779,C929~C932
			13	J1201 PIN2 change to 2.5V
			14	Add R510,R511,R512,R513 as back up of different HCSL OSC
			15	Exchange UART1 and UART2 on CP2105 due to ECI support special input
			16	DNP R909,R910,R911,R912, Install R905,R906,R907,R908
			17	Add L104 FB for PLL to reduce noise
			18	Add R764,Q704,R763 to support over drive mode
B1	2017-07-24	Javen	1	Change WiFi to QCA6174A
			2	Change USB TYPE-C connector
			3	Change R1004,R1009 PU to DCDC_5V_CN
			4	Add C714 to prevent ARM voltage drop when DVFS from 1.0V to 0.9V
			5	DNP R1227
			6	Add R1437,Q1405,R1463,D1403,D403
			7	Change R1459 to PCIe_nDIS
			8	Install R1411,R1442-R1449,C401
			9	Change C913 to 1nF
			10	Change R842 to 1M OHM
			11	DNP C727 add C781 to prevent the power up sequence
B2	2017-08-14	Javen	1	Add C781
			2	Add R1464, D1404, D1405 for WiFi enable backup
			3	DNP D1609 to prevent the SDIO power on later than POR_B
			4	Install R409 4.7K, change R401 to 0 OHM
			5	Add R621 for backup

1. Unless Otherwise Specified:

   All resistors are in ohms, 10%, 1/8 Watt,0603
   All capacitors are in uF, 20%, 50V,0603
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

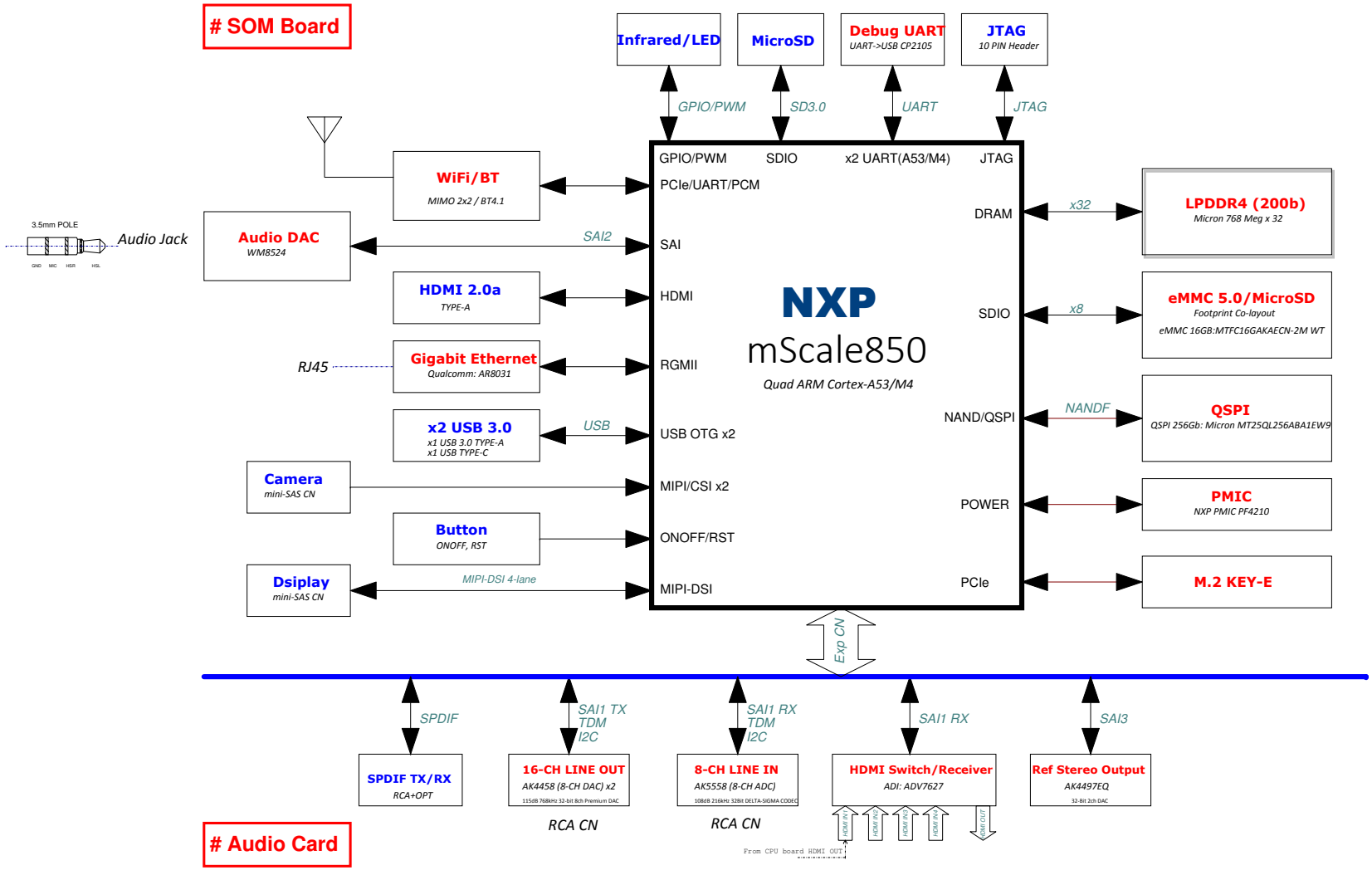
ICAP Classification: CP: IUO: X PUBI:

Designer: <JW>	Drawing Title: mScale850 EVK		
Drawn by: <JW>	Page Title: Title and Rev History		
Approved: <Approver>	Size C	Document Number SCH-29615 PDF: SPF-29615	Rev B1
	Date: Monday, September 25, 2017	Sheet 1 of 23	

mScale850 EVK Block Diagram

Block Diagram Rev 0.6

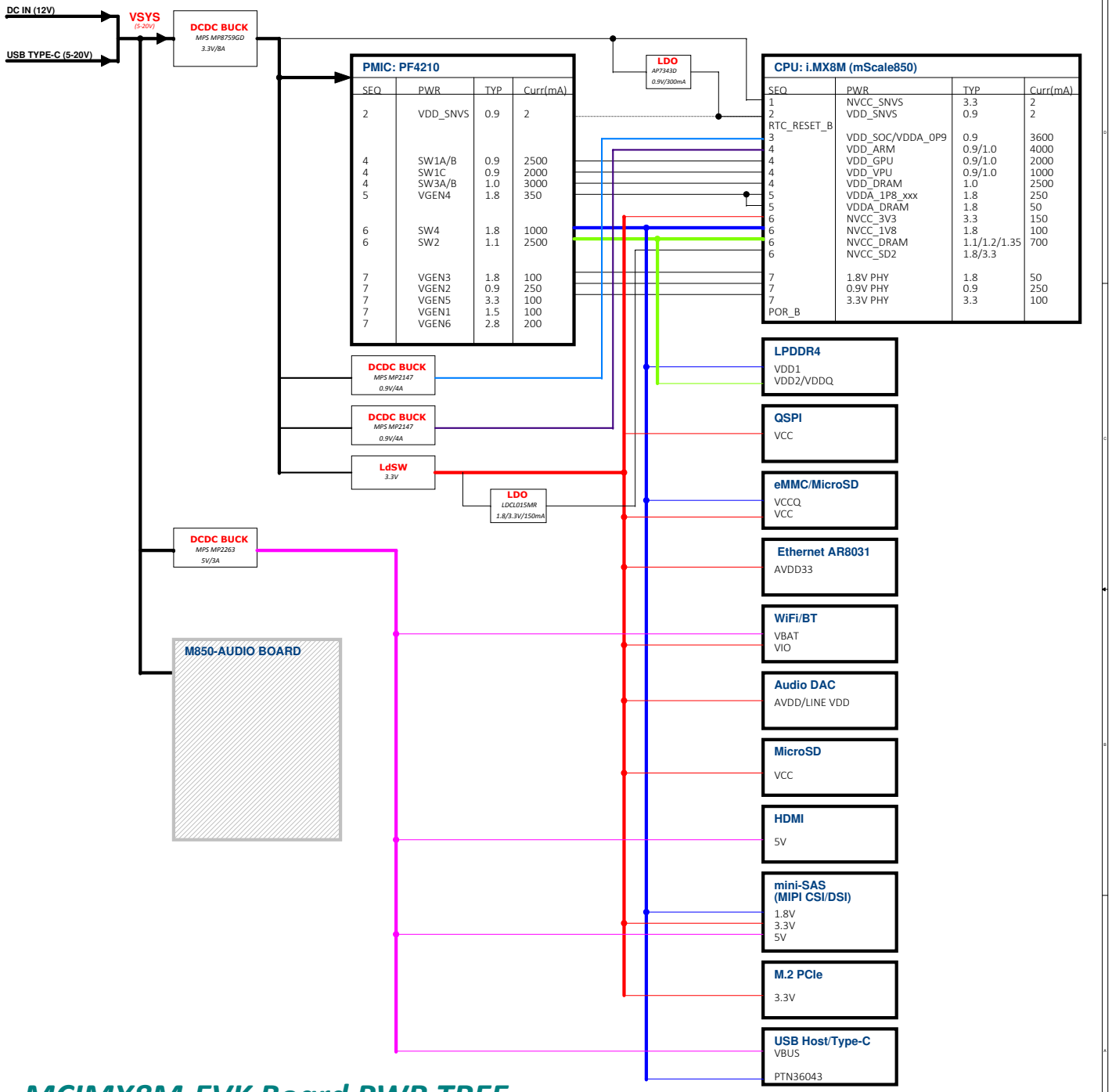
MCIMX8M-EVK
MCIMX8M-AUD



Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: IUO: X PUBI:

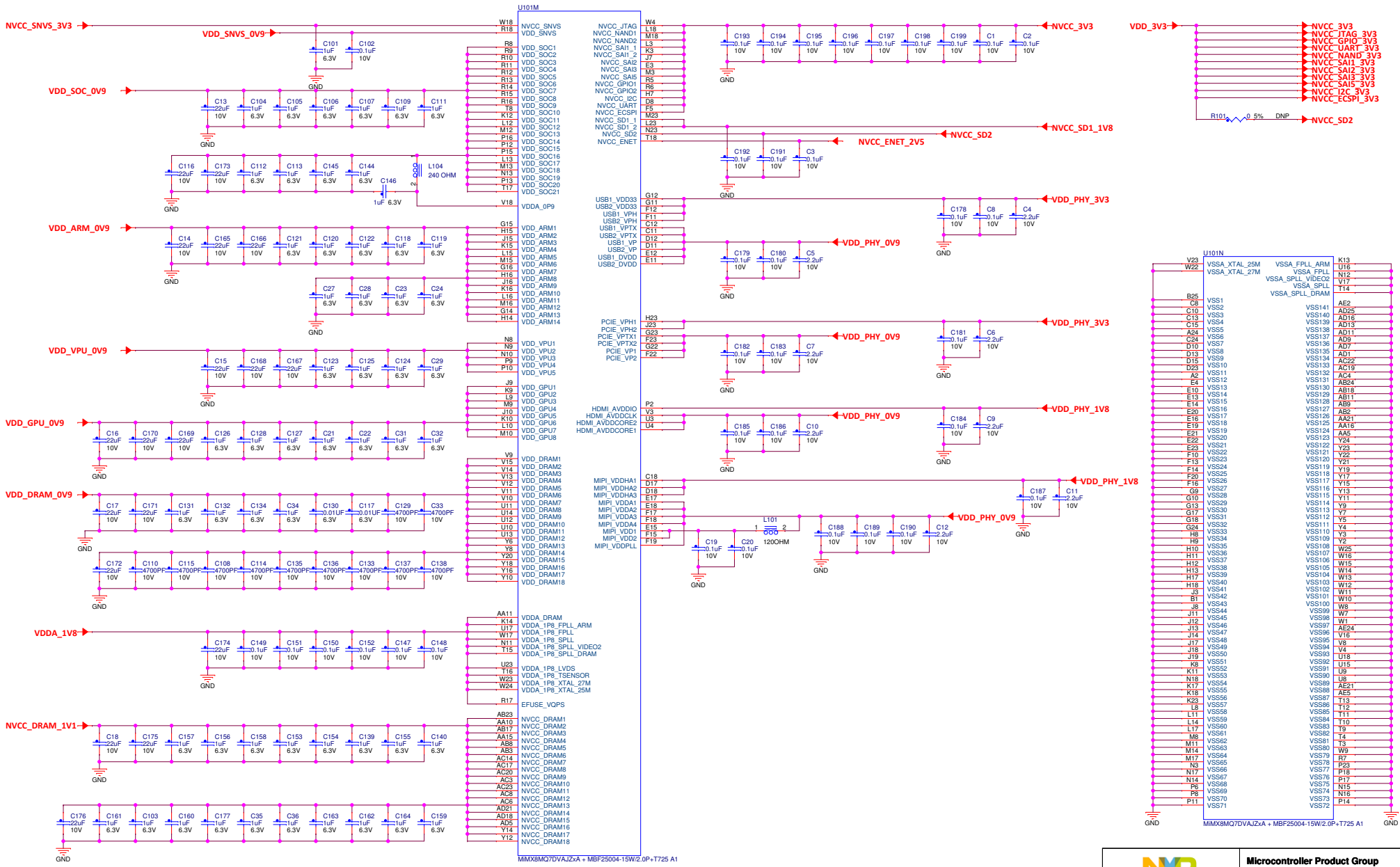
Designer: <JW>	Drawing Title: mScale850 EVK	
Drawn by: <JW>	Page Title: Block Diagram	
Approved: <Approver>	Size C / Document Number SCH-29615 PDF: SPF-29615	Rev B1
	Date: Monday, September 25, 2017	Sheet 2 of 23



MCIMX8M-EVK Board PWR TREE

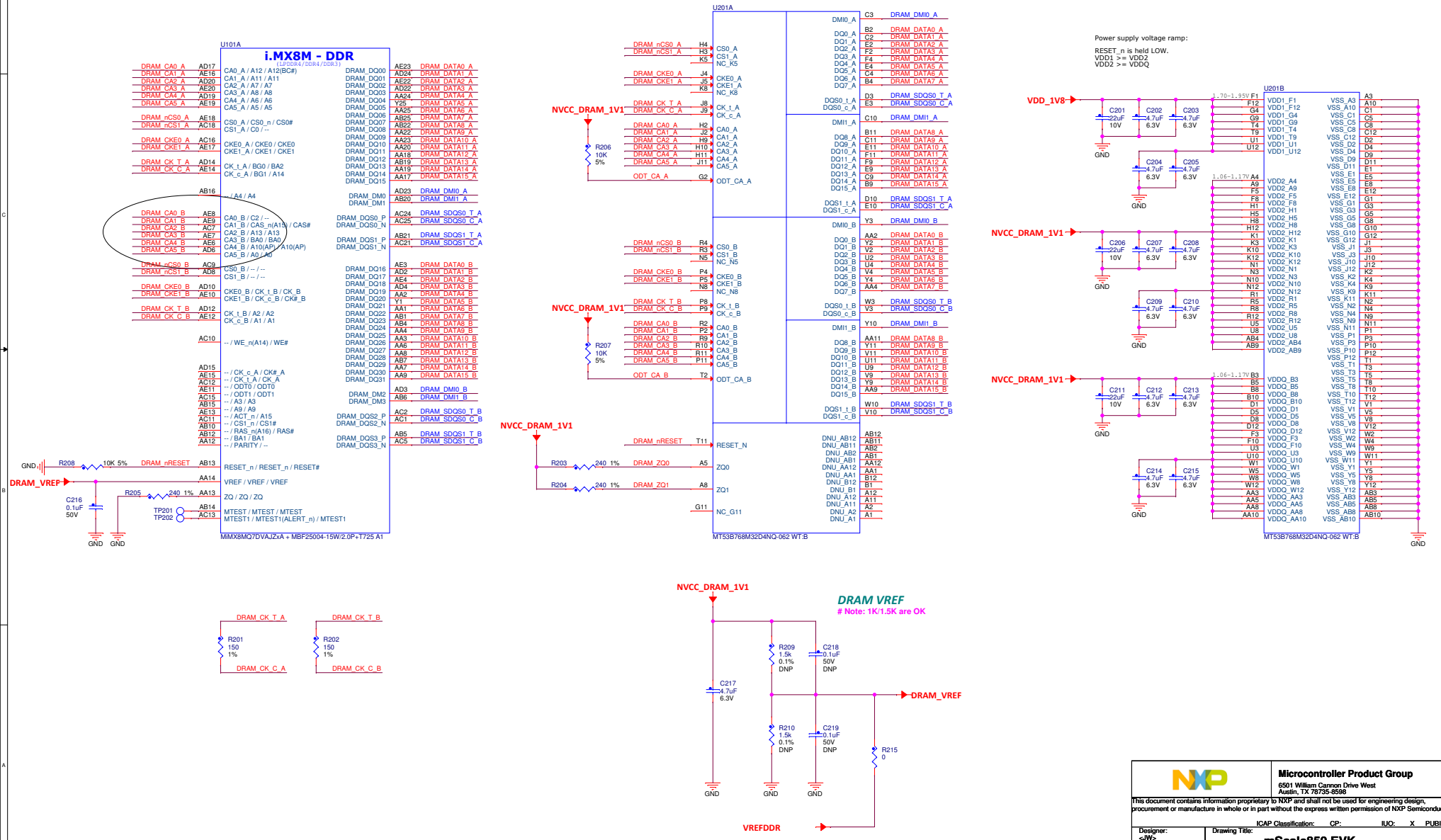
Designer: <JW>	Drawing Title: mScale850 EVK
Drawn by: <JW>	Page Title: Power Tree
Approved: <Approver>	Size: Custom; Document Number: SCH-29815 PDF: SPF-29815; Rev: B1
	Date: Monday, September 25, 2017; Sheet 3 of 23

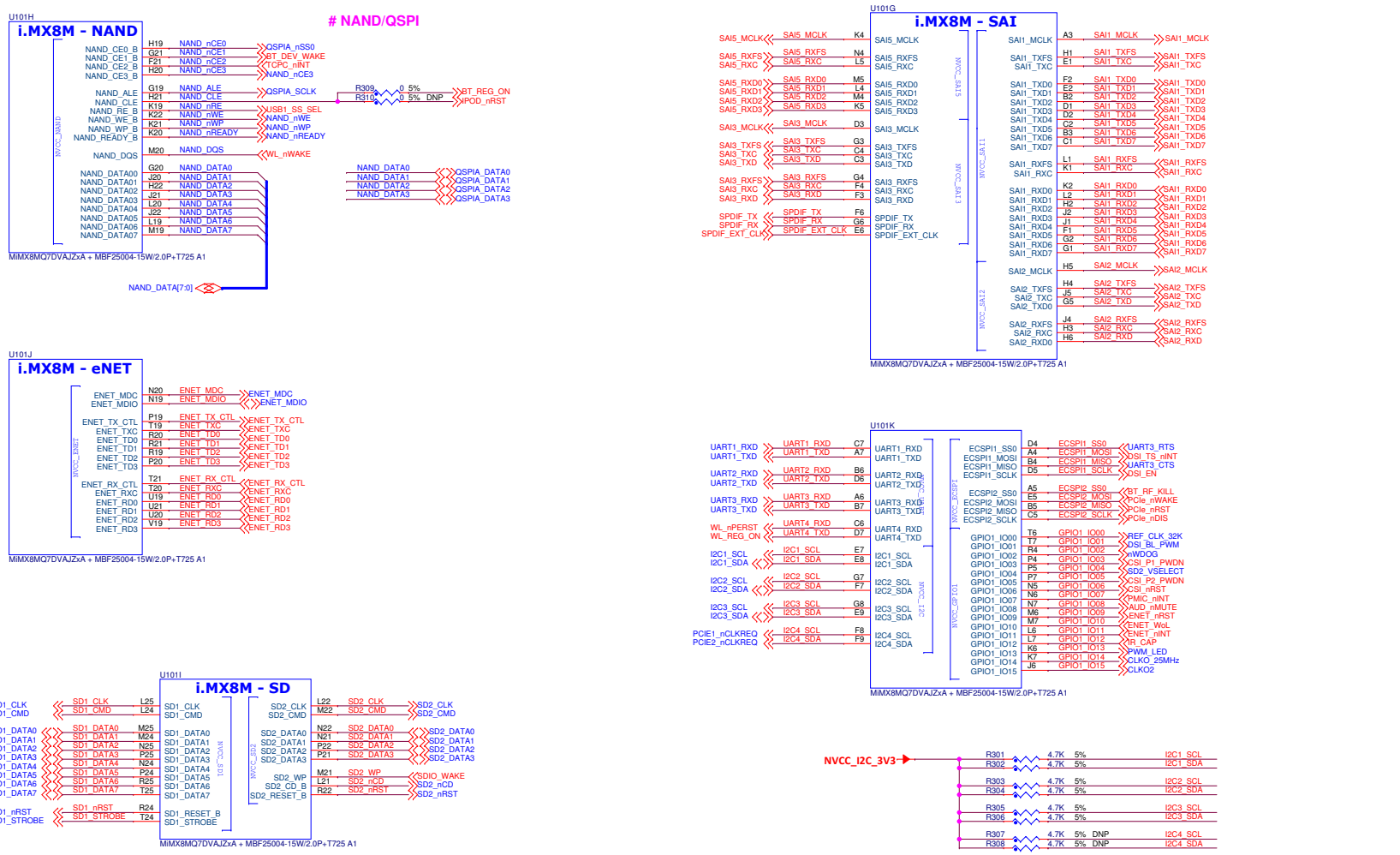
mScale850 PWR

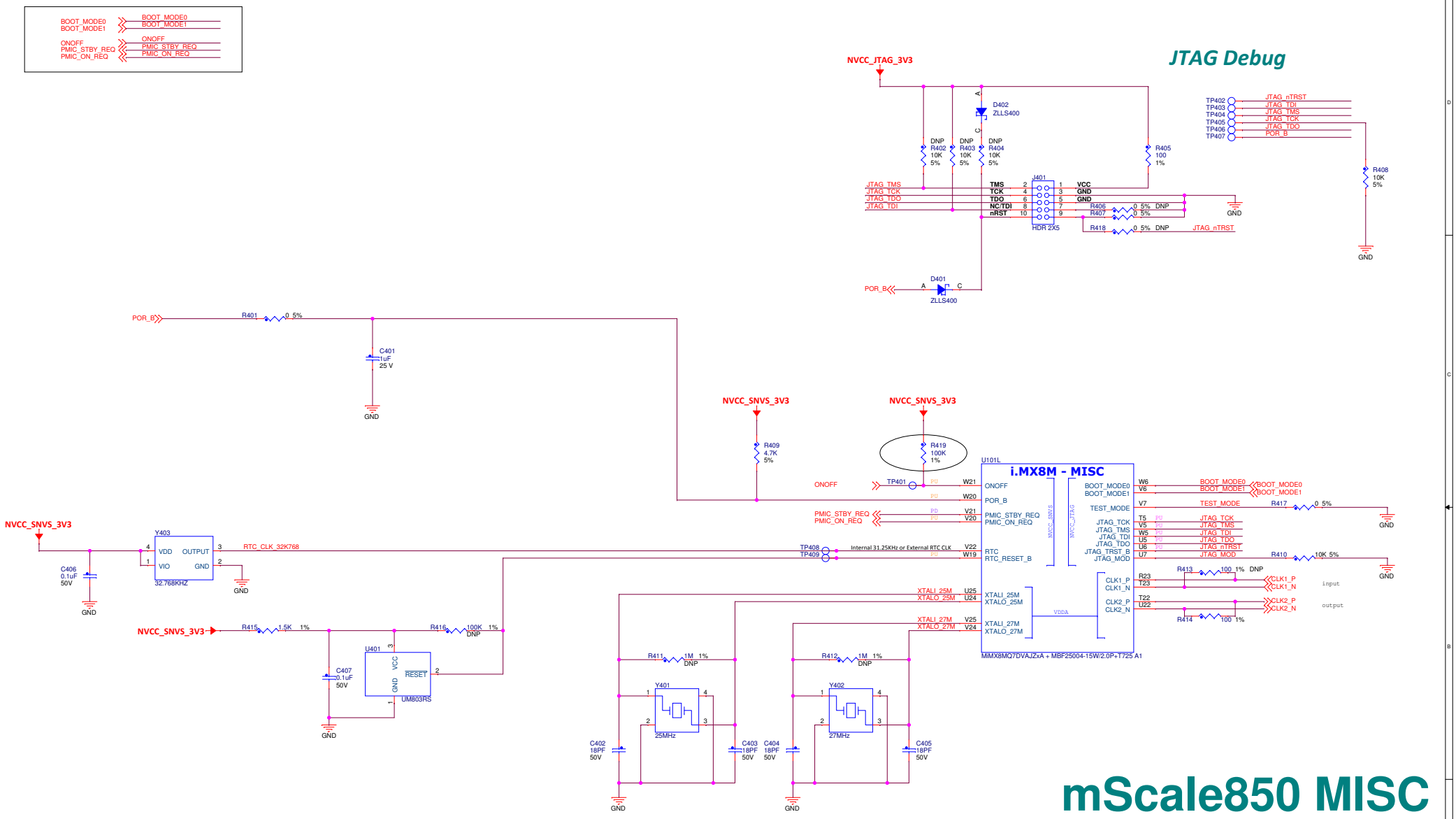


NXP	**Microcontroller Product Group** 6501 William Cannon Drive West Austin, TX 78735-8598	
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.		
ICAP Classification: CP: IUO: X PUBI:		
Designer: <JW>	Drawing Title: **mScale850 EVK**	
Drawn by: <JW>	Page Title: **CPU PWR**	
Approved: <Approver>	Size: C Document Number: SCH-29615 PDF: SPF-29615 Rev: B1	
	Date: Monday, September 25, 2017 Sheet 4 of 23	

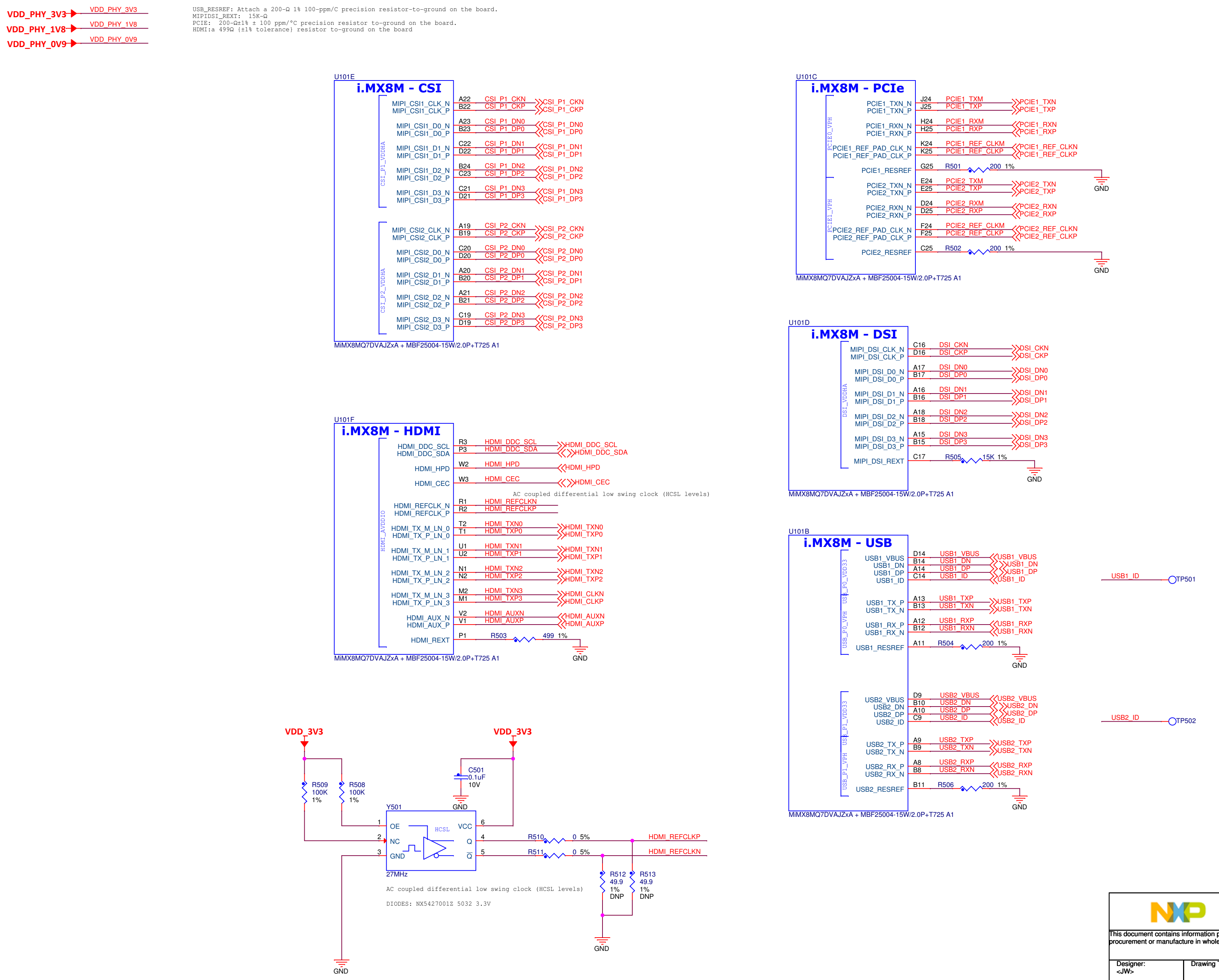
LPDDR4


U101A
i.MX8M - DDR
(LPDDR4/DDR4/DDR3)
MiMX8MQ7DVAJZxA + MBF25004-15W/2.0P+T725 A1
U201A
MT53B768M32D4NQ-062 WT:B
Power supply voltage ramp:
RESET_n is held LOW.
VDD1 >= VDD2
VDD2 >= VDDQ
VDD_1V8
NVCC_DRAM_1V1
DRAM_VREF
VREFDDR
DRAM VREF
Note: 1K/1.5K are OK
Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.
Designer: <JW>
Drawn by: <JW>
Approved: <Approver>
Drawing Title: mScale850 EVK
Page Title: LPDDR4
Size C
Document Number SCH-29615 PDF: SPF-29615
Rev B1
Date: Monday, September 25, 2017
Sheet 5 of 23


-Internal pullup resistors 27 kOhm;
-Internal pulldown resistor of 90kOhm is always enabled
NAND/QSPI
U101H
i.MX8M - NAND
NAND_CE0_B
NAND_CE1_B
NAND_CE2_B
NAND_CE3_B
NAND_ALE
NAND_CLE
NAND_RE_B
NAND_WE_B
NAND_WP_B
NAND_READY_B
NAND_DQS
NAND_DATA00
NAND_DATA01
NAND_DATA02
NAND_DATA03
NAND_DATA04
NAND_DATA05
NAND_DATA06
NAND_DATA07
QSPIA_nSS0
BT_DEV_WAKE
TOPIC_nINT
NAND_nCE3
QSPIA_SCLK
USB1_SS_SEL
NAND_nWE
NAND_nWP
NAND_nREADY
WL_nWAKE
R309
R310
0 5%
0 5% DNP
BT_REG_ON
iPOD_nRST
QSPIA_DATA0
QSPIA_DATA1
QSPIA_DATA2
QSPIA_DATA3
NAND_DATA[7:0]
MiMX8MQ7DVAJZxA + MBF25004-15W/2.0P+T725 A1
U101J
i.MX8M - eNET
ENET_MDC
ENET_MDIO
ENET_TX_CTL
ENET_TXC
ENET_TD0
ENET_TD1
ENET_TD2
ENET_TD3
ENET_RX_CTL
ENET_RXC
ENET_RD0
ENET_RD1
ENET_RD2
ENET_RD3
MiMX8MQ7DVAJZxA + MBF25004-15W/2.0P+T725 A1
U101I
i.MX8M - SD
SD1_CLK
SD1_CMD
SD1_DATA0
SD1_DATA1
SD1_DATA2
SD1_DATA3
SD1_DATA4
SD1_DATA5
SD1_DATA6
SD1_DATA7
SD1_nRST
SD1_STROBE
SD2_CLK
SD2_CMD
SD2_DATA0
SD2_DATA1
SD2_DATA2
SD2_DATA3
SD2_WP
SD2_CD_B
SD2_RESET_B
SDIO_WAKE
SD2_nCD
SD2_nRST
MiMX8MQ7DVAJZxA + MBF25004-15W/2.0P+T725 A1
U101G
i.MX8M - SAI
SAI5_MCLK
SAI5_RXFS
SAI5_RXC
SAI5_RXD0
SAI5_RXD1
SAI5_RXD2
SAI5_RXD3
SAI3_MCLK
SAI3_TXFS
SAI3_TXC
SAI3_TXD
SAI3_RXFS
SAI3_RXC
SAI3_RXD
SPDIF_TX
SPDIF_RX
SPDIF_EXT_CLK
SAI1_MCLK
SAI1_TXFS
SAI1_TXC
SAI1_TXD0
SAI1_TXD1
SAI1_TXD2
SAI1_TXD3
SAI1_TXD4
SAI1_TXD5
SAI1_TXD6
SAI1_TXD7
SAI1_RXFS
SAI1_RXC
SAI1_RXD0
SAI1_RXD1
SAI1_RXD2
SAI1_RXD3
SAI1_RXD4
SAI1_RXD5
SAI1_RXD6
SAI1_RXD7
SAI2_MCLK
SAI2_TXFS
SAI2_TXC
SAI2_TXD0
SAI2_RXFS
SAI2_RXC
SAI2_RXD0
MiMX8MQ7DVAJZxA + MBF25004-15W/2.0P+T725 A1
U101K
UART1_RXD
UART1_TXD
UART2_RXD
UART2_TXD
UART3_RXD
UART3_TXD
UART4_RXD
UART4_TXD
WL_nPERST
WL_REG_ON
I2C1_SCL
I2C1_SDA
I2C2_SCL
I2C2_SDA
I2C3_SCL
I2C3_SDA
I2C4_SCL
I2C4_SDA
PCIE1_nCLKREQ
PCIE2_nCLKREQ
ECSPI1_SS0
ECSPI1_MOSI
ECSPI1_MISO
ECSPI1_SCLK
ECSPI2_SS0
ECSPI2_MOSI
ECSPI2_MISO
ECSPI2_SCLK
GPIO1_IO00
GPIO1_IO01
GPIO1_IO02
GPIO1_IO03
GPIO1_IO04
GPIO1_IO05
GPIO1_IO06
GPIO1_IO07
GPIO1_IO08
GPIO1_IO09
GPIO1_IO10
GPIO1_IO11
GPIO1_IO12
GPIO1_IO13
GPIO1_IO14
GPIO1_IO15
UART3_RTS
DSI_TS_nINT
UART3_CTS
DSI_EN
BT_RF_KILL
PCIe_nWAKE
PCIe_nRST
PCIe_nDIS
REF_CLK_32K
DSI_BL_PWM
nWDOG
CSI_P1_PWDN
SD2_VSELECT
CSI_P2_PWDN
CSI_nRST
PMIC_nINT
AUD_nMUTE
ENET_nRST
ENET_WoL
ENET_nINT
IR_CAP
PWM_LED
CLKO_25MHz
CLKO2
NVCC_I2C_3V3
R301
R302
R303
R304
R305
R306
R307
R308
4.7K 5%
4.7K 5% DNP
I2C1_SCL
I2C1_SDA
I2C2_SCL
I2C2_SDA
I2C3_SCL
I2C3_SDA
I2C4_SCL
I2C4_SDA
Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.
ICAP Classification: CP: IUO: X PUBI:
Designer: <JW>
Drawing Title: mScale850 EVK
Drawn by: <JW>
Page Title: CPU IO
Approved: <Approver>
Size C
Document Number SCH-29615 PDF: SPF-29615
Rev B1
Date: Monday, September 25, 2017
Sheet 6 of 23


BOOT_MODE0
BOOT_MODE1
ONOFF
PMIC_STBY_REQ
PMIC_ON_REQ
JTAG Debug
NVCC_JTAG_3V3
D402
ZLLS400
DNP R402 10K 5%
DNP R403 10K 5%
DNP R404 10K 5%
R405 100 1%
R408 10K 5%
TP402
TP403
TP404
TP405
TP406
TP407
JTAG_nTRST
JTAG_TDI
JTAG_TMS
JTAG_TCK
JTAG_TDO
POR_B
J401
HDR 2X5
R406 0 5% DNP
R407 0 5%
R418 0 5% DNP
D401
ZLLS400
GND
POR_B
R401 0 5%
C401 1uF 25 V
NVCC_SNVS_3V3
R409 4.7K 5%
R419 100K 1%
U101L
i.MX8M - MISC
ONOFF
POR_B
PMIC_STBY_REQ
PMIC_ON_REQ
RTC
RTC_RESET_B
BOOT_MODE0
BOOT_MODE1
TEST_MODE
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST_B
JTAG_MOD
CLK1_P
CLK1_N
CLK2_P
CLK2_N
XTALI_25M
XTALO_25M
XTALI_27M
XTALO_27M
VDDA
R417 0 5%
R410 10K 5%
R413 100 1% DNP
R414 100 1%
input
output
MiMX8MQ7DVAJZxA + MBF25004-15W/2.0P+T725 A1
NVCC_SNVS_3V3
Y403
32.768KHZ
C406 0.1uF 50V
RTC_CLK_32K768
Internal 31.25KHz or External RTC CLK
TP408
TP409
R415 1.5K 1%
R416 100K 1% DNP
U401
UM803RS
C407 0.1uF 50V
R411 1M 1% DNP
R412 1M 1% DNP
Y401
25MHz
Y402
27MHz
C402 18PF 50V
C403 18PF 50V
C404 18PF 50V
C405 18PF 50V
mScale850 MISC
Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.
ICAP Classification: CP: IUO: X PUBI:
Designer: <JW>
Drawn by: <JW>
Approved: <Approver>
Drawing Title: mScale850 EVK
Page Title: CPU PERI2
Size C
Document Number SCH-29615 PDF: SPF-29615
Rev B1
Date: Monday, September 25, 2017
Sheet 7 of 23

mScale850 PHY



VDD_PHY_3V3
VDD_PHY_1V8
VDD_PHY_0V9
USB_RESREF: Attach a 200-Ω 1% 100-ppm/C precision resistor-to-ground on the board.
MIPIDSI_REXT: 15K-Ω
PCIE: 200-Ω±1% ± 100 ppm/°C precision resistor to-ground on the board.
HDMI:a 499Ω (±1% tolerance) resistor to-ground on the board
U101E
i.MX8M - CSI
MIPI_CSI1_CLK_N MIPI_CSI1_CLK_P MIPI_CSI1_D0_N MIPI_CSI1_D0_P MIPI_CSI1_D1_N MIPI_CSI1_D1_P MIPI_CSI1_D2_N MIPI_CSI1_D2_P MIPI_CSI1_D3_N MIPI_CSI1_D3_P
CSI_P1_VDDHA
MIPI_CSI2_CLK_N MIPI_CSI2_CLK_P MIPI_CSI2_D0_N MIPI_CSI2_D0_P MIPI_CSI2_D1_N MIPI_CSI2_D1_P MIPI_CSI2_D2_N MIPI_CSI2_D2_P MIPI_CSI2_D3_N MIPI_CSI2_D3_P
CSI_P2_VDDHA
CSI_P1_CKN CSI_P1_CKP CSI_P1_DN0 CSI_P1_DP0 CSI_P1_DN1 CSI_P1_DP1 CSI_P1_DN2 CSI_P1_DP2 CSI_P1_DN3 CSI_P1_DP3
CSI_P2_CKN CSI_P2_CKP CSI_P2_DN0 CSI_P2_DP0 CSI_P2_DN1 CSI_P2_DP1 CSI_P2_DN2 CSI_P2_DP2 CSI_P2_DN3 CSI_P2_DP3
MIMX8MQ7DVAJZxA + MBF25004-15W/2.0P+T725 A1
U101C
i.MX8M - PCIe
PCIE1_TXN_N PCIE1_TXN_P PCIE1_RXN_N PCIE1_RXN_P PCIE1_REF_PAD_CLK_N PCIE1_REF_PAD_CLK_P PCIE1_RESREF
PCIE2_TXN_N PCIE2_TXN_P PCIE2_RXN_N PCIE2_RXN_P PCIE2_REF_PAD_CLK_N PCIE2_REF_PAD_CLK_P PCIE2_RESREF
PCIE0_VPH PCIE1_VPH
PCIE1_TXM PCIE1_TXP PCIE1_RXM PCIE1_RXP PCIE1_REF_CLKM PCIE1_REF_CLKP
R501 200 1% GND
PCIE2_TXM PCIE2_TXP PCIE2_RXM PCIE2_RXP PCIE2_REF_CLKM PCIE2_REF_CLKP
R502 200 1% GND
PCIE1_TXN PCIE1_TXP PCIE1_RXN PCIE1_RXP PCIE1_REF_CLKN PCIE1_REF_CLKP PCIE2_TXN PCIE2_TXP PCIE2_RXN PCIE2_RXP PCIE2_REF_CLKN PCIE2_REF_CLKP
MIMX8MQ7DVAJZxA + MBF25004-15W/2.0P+T725 A1
U101D
i.MX8M - DSI
MIPI_DSI_CLK_N MIPI_DSI_CLK_P MIPI_DSI_D0_N MIPI_DSI_D0_P MIPI_DSI_D1_N MIPI_DSI_D1_P MIPI_DSI_D2_N MIPI_DSI_D2_P MIPI_DSI_D3_N MIPI_DSI_D3_P MIPI_DSI_REXT
DSI_VDDHA
DSI_CKN DSI_CKP DSI_DN0 DSI_DP0 DSI_DN1 DSI_DP1 DSI_DN2 DSI_DP2 DSI_DN3 DSI_DP3
R505 15K 1% GND
MIMX8MQ7DVAJZxA + MBF25004-15W/2.0P+T725 A1
U101F
i.MX8M - HDMI
HDMI_DDC_SCL HDMI_DDC_SDA HDMI_HPD HDMI_CEC HDMI_REFCLK_N HDMI_REFCLK_P HDMI_TX_M_LN_0 HDMI_TX_P_LN_0 HDMI_TX_M_LN_1 HDMI_TX_P_LN_1 HDMI_TX_M_LN_2 HDMI_TX_P_LN_2 HDMI_TX_M_LN_3 HDMI_TX_P_LN_3 HDMI_AUX_N HDMI_AUX_P HDMI_REXT
HDMI_AVDDIO
AC coupled differential low swing clock (HCSL levels)
HDMI_REFCLKN HDMI_REFCLKP
HDMI_TXN0 HDMI_TXP0 HDMI_TXN1 HDMI_TXP1 HDMI_TXN2 HDMI_TXP2 HDMI_TXN3 HDMI_TXP3 HDMI_CLKN HDMI_CLKP HDMI_AUXN HDMI_AUXP
R503 499 1% GND
MIMX8MQ7DVAJZxA + MBF25004-15W/2.0P+T725 A1
U101B
i.MX8M - USB
USB1_VBUS USB1_DN USB1_DP USB1_ID USB1_TX_P USB1_TX_N USB1_RX_P USB1_RX_N USB1_RESREF
USB_P0_VDD33 USB_P0_VPH
USB1_VBUS USB1_DN USB1_DP USB1_ID USB1_TXP USB1_TXN USB1_RXP USB1_RXN
R504 200 1% GND
USB1_ID TP501
USB2_VBUS USB2_DN USB2_DP USB2_ID USB2_TX_P USB2_TX_N USB2_RX_P USB2_RX_N USB2_RESREF
USB_P1_VDD33 USB_P1_VPH
USB2_VBUS USB2_DN USB2_DP USB2_ID USB2_TXP USB2_TXN USB2_RXP USB2_RXN
R506 200 1% GND
USB2_ID TP502
MIMX8MQ7DVAJZxA + MBF25004-15W/2.0P+T725 A1
VDD_3V3
VDD_3V3
R509 100K 1%
R508 100K 1%
C501 0.1uF 10V
GND
Y501
OE NC GND VCC Q
HCSL
27MHz
R510 0 5%
R511 0 5%
HDMI_REFCLKP
HDMI_REFCLKN
R512 49.9 1% DNP
R513 49.9 1% DNP
GND
GND
AC coupled differential low swing clock (HCSL levels)
DIODES: NX5427001Z 5032 3.3V

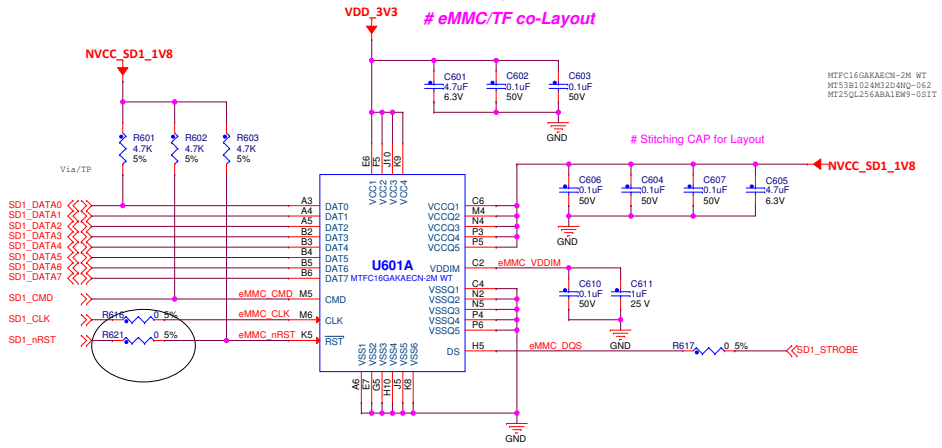
Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.

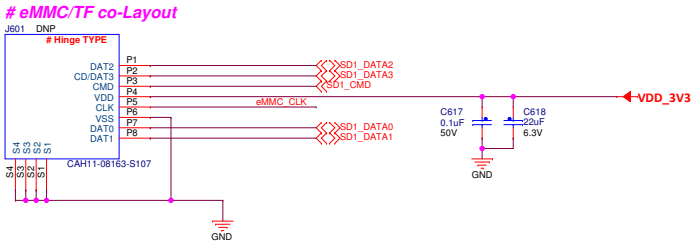
ICAP Classification: CP: ___ IUO: X PUBI: ___

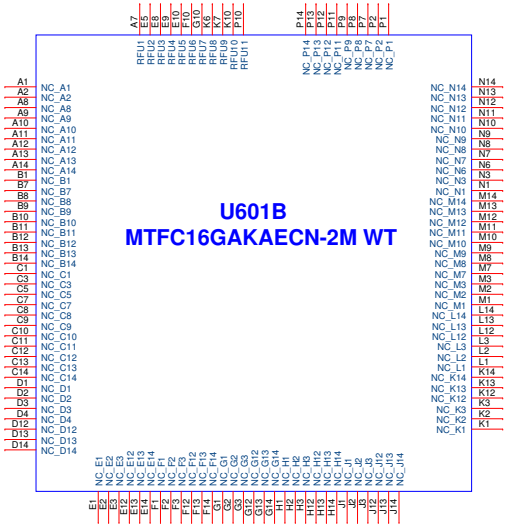
Designer: <JW>	Drawing Title: mScale850 EVK	
Drawn by: <JW>	Page Title: CPU PHY	
Approved: <Approver>	Size C / Document Number SCH-29615 PDF: SPF-29615	Rev B1
	Date: Monday, September 25, 2017	Sheet 8 of 23

eMMC 5.0 Footprint

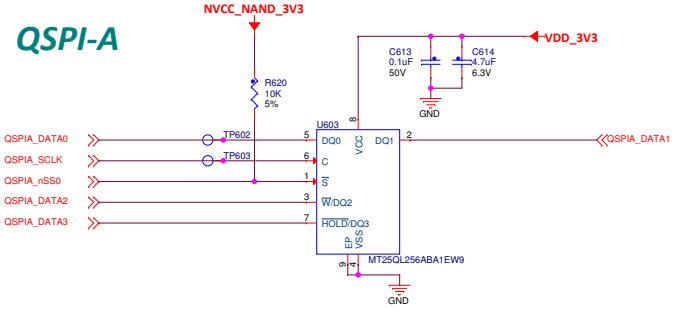


Hinge Type MicroSD





QSPI-A



Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

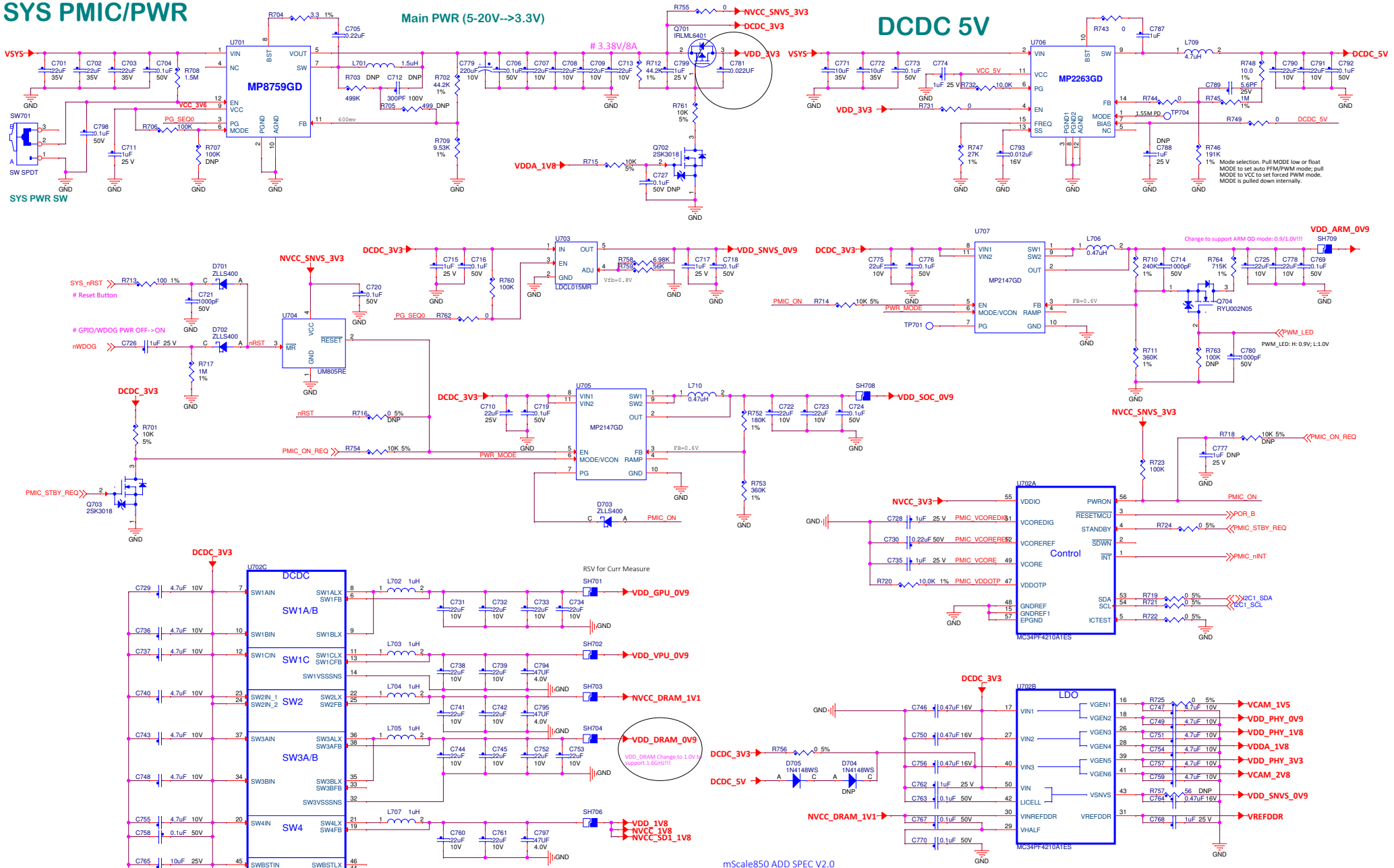
ICAP Classification: CP: IUO: X PUBI:

Designer: <JW>	Drawing Title: mScale850 EVK		
Drawn by: <JW>	Page Title: Flash		
Approved: <Approver>	Size C	Document Number SCH-29615 PDF: SPF-29615	Rev B1
	Date: Monday, September 25, 2017	Sheet 9 of 23	

SYS PMIC/PWR

Main PWR (5-20V-->3.3V)

DCDC 5V



mScale850 ADD SPEC V2.0

SEQ	PWR	MIN	TYP	MAX	Curr(mA)
1	NVCC_SNVS	3	3.3	3.6	2
2	VDD_SNVS	0.81	0.9	0.99	2
RTC_RESET_B					
3	VDD_SOC/VDDA_0P9	0.81	0.9	0.99	3600
4	VDD_GPU	0.81	0.9/1.0	1.1	2000
4	VDD_VPU	0.81	0.9/1.0	1.1	1000
4	VDD_DRAM	0.81	1.0	1.05	2500
4	VDD_ARM	0.81	0.9/1.0	1.1	4000
5	VDDA_1P8_xxx	1.62	1.8	1.89	250
5	VDDA_DRAM	1.71	1.8	1.89	50
6	NVCC_DRAM		1.1/1.2/1.35		2170
6	NVCC_3V3	3	3.3	3.6	100
6	NVCC_1V8	1.65	1.8	1.95	450
7	3.3V PHY	3.069	3.3	3.63	100
7	1.8V PHY	1.674	1.8	1.98	50
7	0.9V PHY	0.837	0.9	0.99	250
POR_B					

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: IUO: X PUBI:

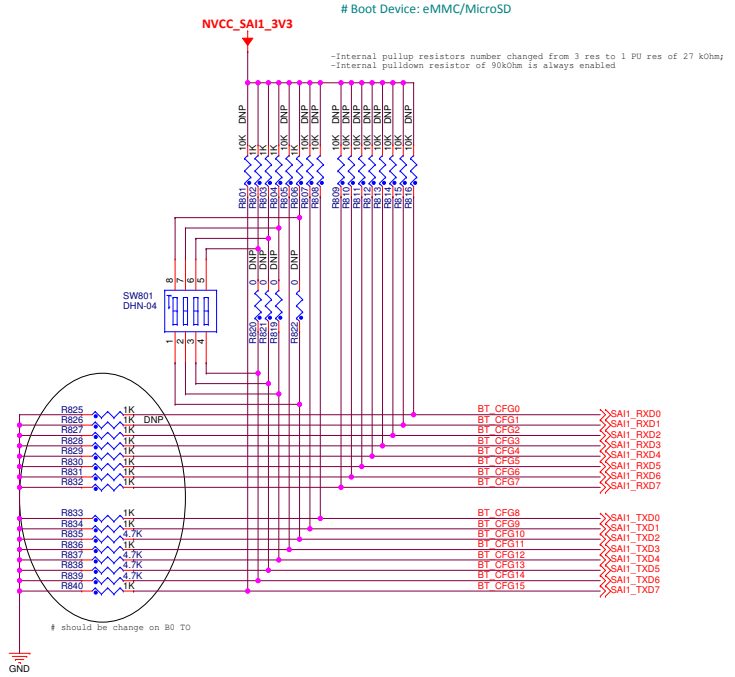
Designer: <JW>	Drawing Title: mScale850 EVK		
Drawn by: <JW>	Page Title: PMIC		
Approved: <Approver>	Size: C	Document Number: SCH-29615 PDF: SPF-29615	Rev: B1
	Date: Wednesday, September 27, 2017	Sheet 10 of 23	

mScale 8Quad Boot ROM Fuse <Default: QSPI BOOT>

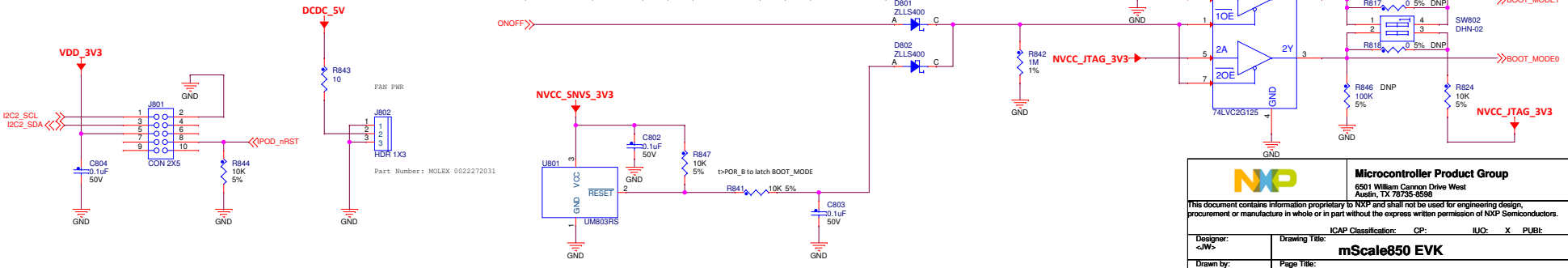
	Address	7	6	5	4	3	2	1	0
	0x470[15:8]	BOOT_CFG[15]	BOOT_CFG[14]	BOOT_CFG[13]	BOOT_CFG[12]	BOOT_CFG[11]	BOOT_CFG[10]	BOOT_CFG[9]	BOOT_CFG[8]
	0x470[15:8]	Infinit-Loop (Debug USE only) 0 - Disable 1 - Enable	001 - SD/eSD			Port Select: 00 - eSDHC1 01 - eSDHC2		Power Cycle Enable '0' - No power cycle '1' - Enabled via	SD Loopback Clock Source Sel (for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
	0x470[15:8]		010 - MMC/eMMC						
	0x470[15:8]		011 - NAND			Pages In Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5	
	0x470[15:8]		100 - QSPI			QSPI Instance 0 - QuadSPI0 1 - Reserved	SDR SMP: "000" : Default "001-111"		
	0x470[15:8]		110 - SPI NOR			Port Select: 000 - eCSPI1 001 - eCSPI2			SPI Addressing: 0 - 3-bytes (24-bit) 1 - 2-bytes (16-bit)
	0x470[15:8]	Others - Reserved for future use							
		BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]	BOOT_CFG[1]	BOOT_CFG[0]
SD/eSD	0x470[7:0]	Fast Boot: 0 - Regular 1 - Fast Boot	Reserved	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	Speed 000 - Normal/SDR12 001 - High/SDR25 010 - SDR50 011 - SDR104 101 - Reserved for DDR50 Others - Reserved			Reserved
MMC/eMMC	0x470[7:0]		Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved.			Speed 00 - Normal 01 - High 10 - Reserved for HS200 11 - Reserved		USDHC1 IO VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	USDHC2 IO VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V
NAND	0x470[7:0]	BT_TOGGLEMODE	BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles. '1111'- 15 GPMICLK cycles.			Reserved
QSPI	0x470[7:0]	HSPHS: Half Speed Phase Selection 0 : select sampling at non-inverted clock 1: select sampling at inverted clock	HSDLY: Half Speed Delay selection 0 : one clock delay 1: two clock delay	FSPHS: Full Speed Phase Selection 0 : select sampling at non-inverted clock 1: select sampling at inverted clock	FSDLY: Full Speed Delay selection 0 : one clock delay 1: two clock delay	Reserved	Reserved	Reserved	Reserved
SPINOR	0x470[7:0]	CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

BMODE[1:0]	BOOT TYPE
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot (Development)
11	Reserved

Boot Device: eMMC/MicroSD



item	Power state	ONOFF	RST	OE	DIP SW	BM1	BM0	Note	Description
1	During Power Up	H (No press)	L	H	1-4 : OFF; 2-3 : ON	0	1	Serial Downloader	item 1/2 for system development
2	During Power Up	H (No press)	L	H	1-4 : ON; 2-3 : OFF	1	0	Internal Boot	item 2/3 for system upgrade
3	During Power Up	L (Press)	L	L	1-4 : ON; 2-3 : OFF	0	1	Serial Downloader	
4	After Power Up	H (No press)	H	H	/	/	/	No power key event	Normal power key function
5	After Power Up	L (Short Press)	H	H	/	/	/	Power key event	
6	After Power Up	L (Long Press)	H	H	/	/	/	System power down	

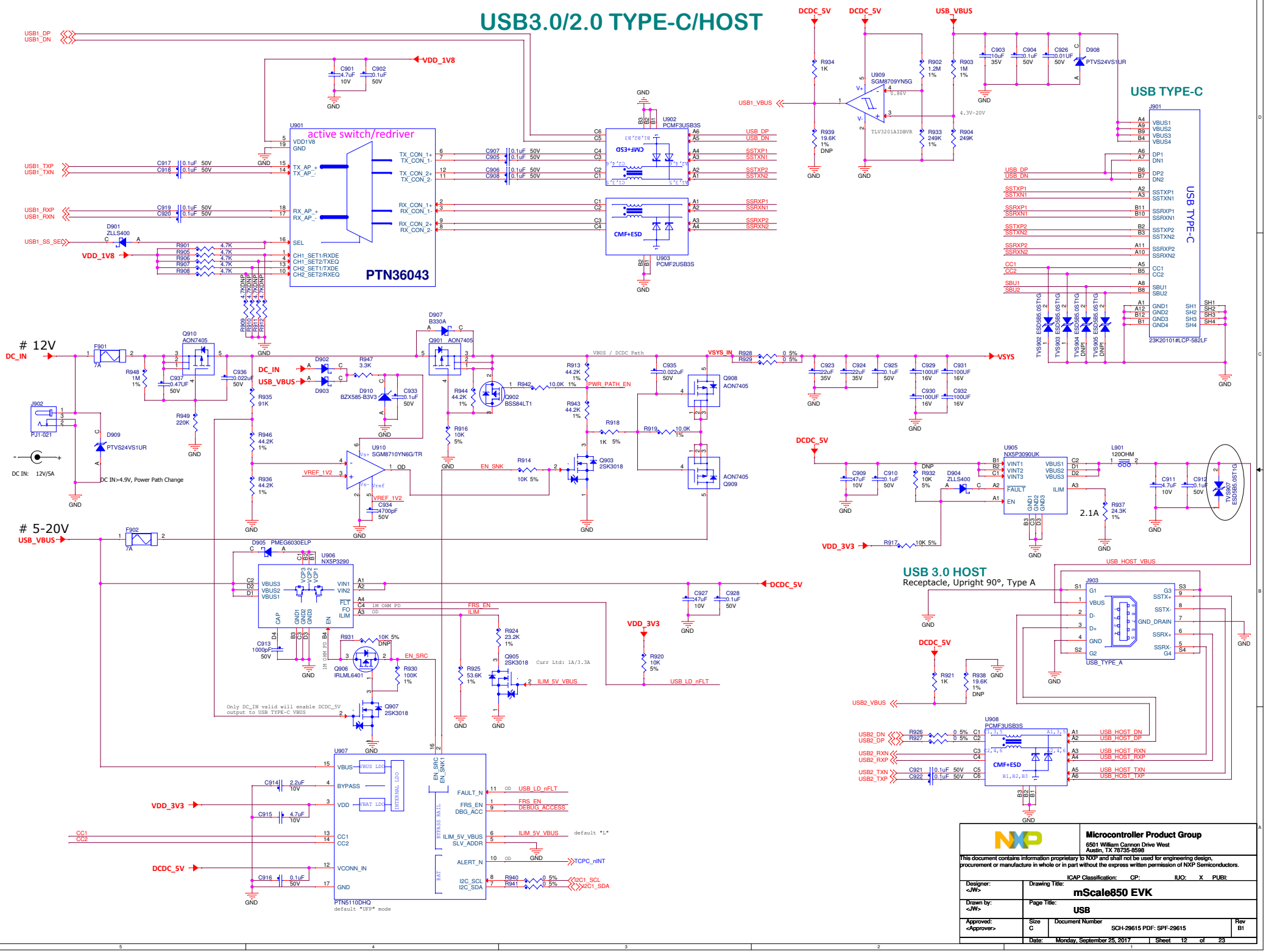


Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: IUO: X PUBI:

Designer: <JW>	Drawing Title: mScale850 EVK	
Drawn by: <JW>	Page Title: BOOT_CFG	
Approved: <Approver>	Size C	Document Number SCH-29615 PDF: SPF-29615 Rev B1
	Date: Monday, September 25, 2017	Sheet 11 of 23

USB3.0/2.0 TYPE-C/HOST



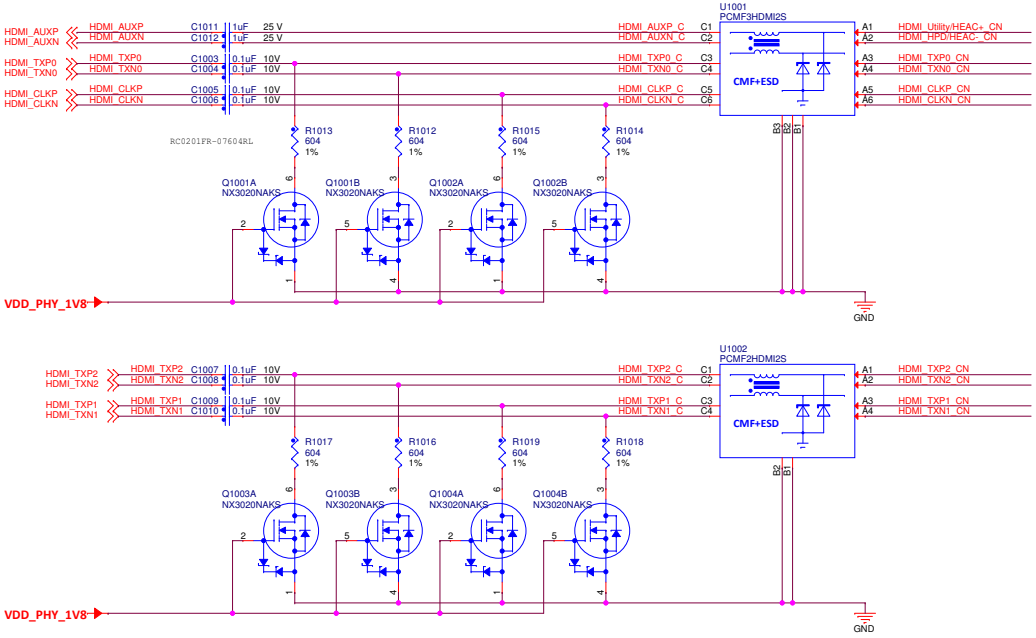
NXP	**Microcontroller Product Group**	
	6501 William Cannon Drive West Austin, TX 78735-8598	

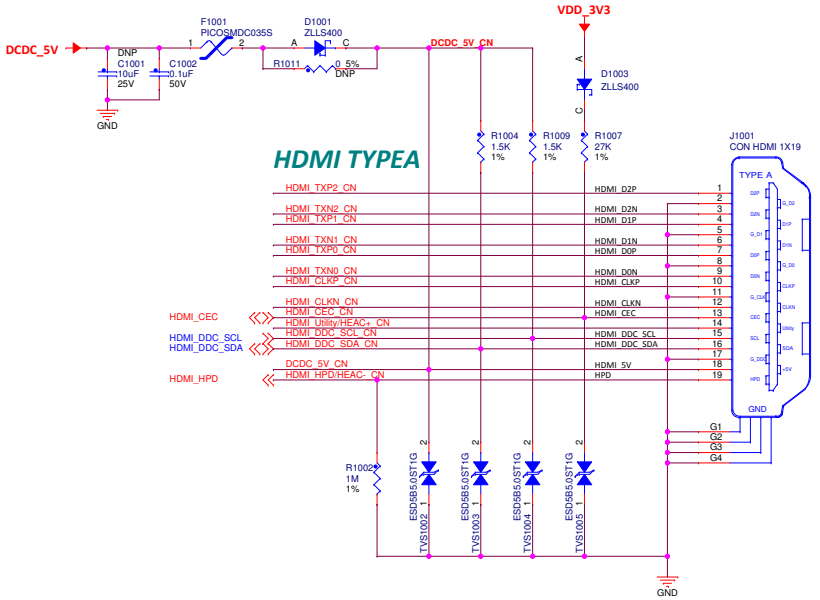
ICAP Classification: CP: IUO: X PUBI:

Designer: <JW>	Drawing Title: **mScale850 EVK**	
Drawn by: <JW>	Page Title: **USB**	
Approved: <Approver>	Size: C	Document Number: SCH-29615 PDF: SPF-29615 Rev: B1
	Date: Monday, September 25, 2017	Sheet 12 of 23

HDMI 2.0a TX

HDMI data EMI/ESD

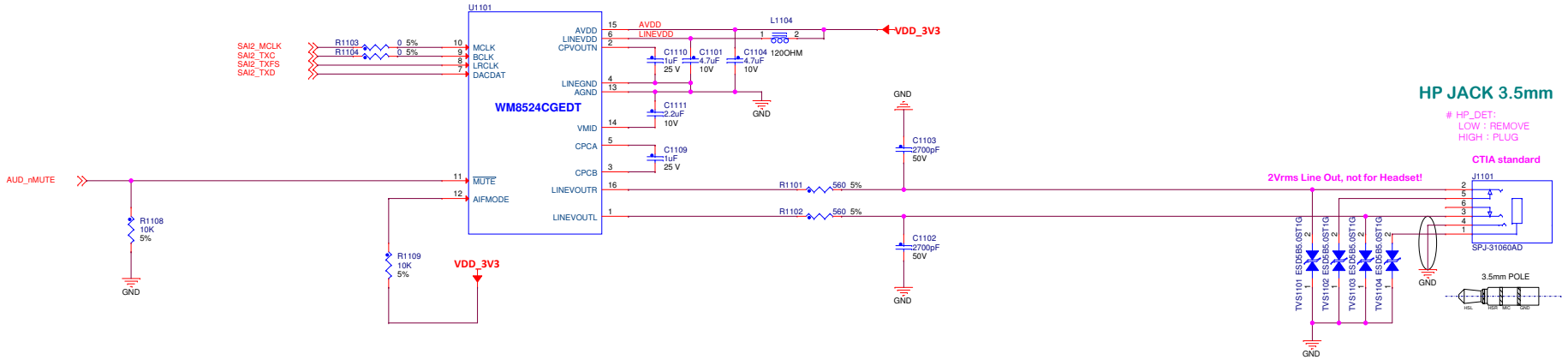




NXP	Microcontroller Product Group 6501 William Cannon Drive West Austin, TX 78735-8598	
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.		
	ICAP Classification: CP: IUO: X PUBI:	
Designer: <JW>	Drawing Title: mScale850 EVK	
Drawn by: <JW>	Page Title: HDMI	
Approved: <Approver>	Size C / Document Number SCH-29615 PDF: SPF-29615	Rev B1
	Date: Monday, September 25, 2017	Sheet 13 of 23

Audio DAC

24-bit 192kHz Stereo DAC 2Vrms Line Out

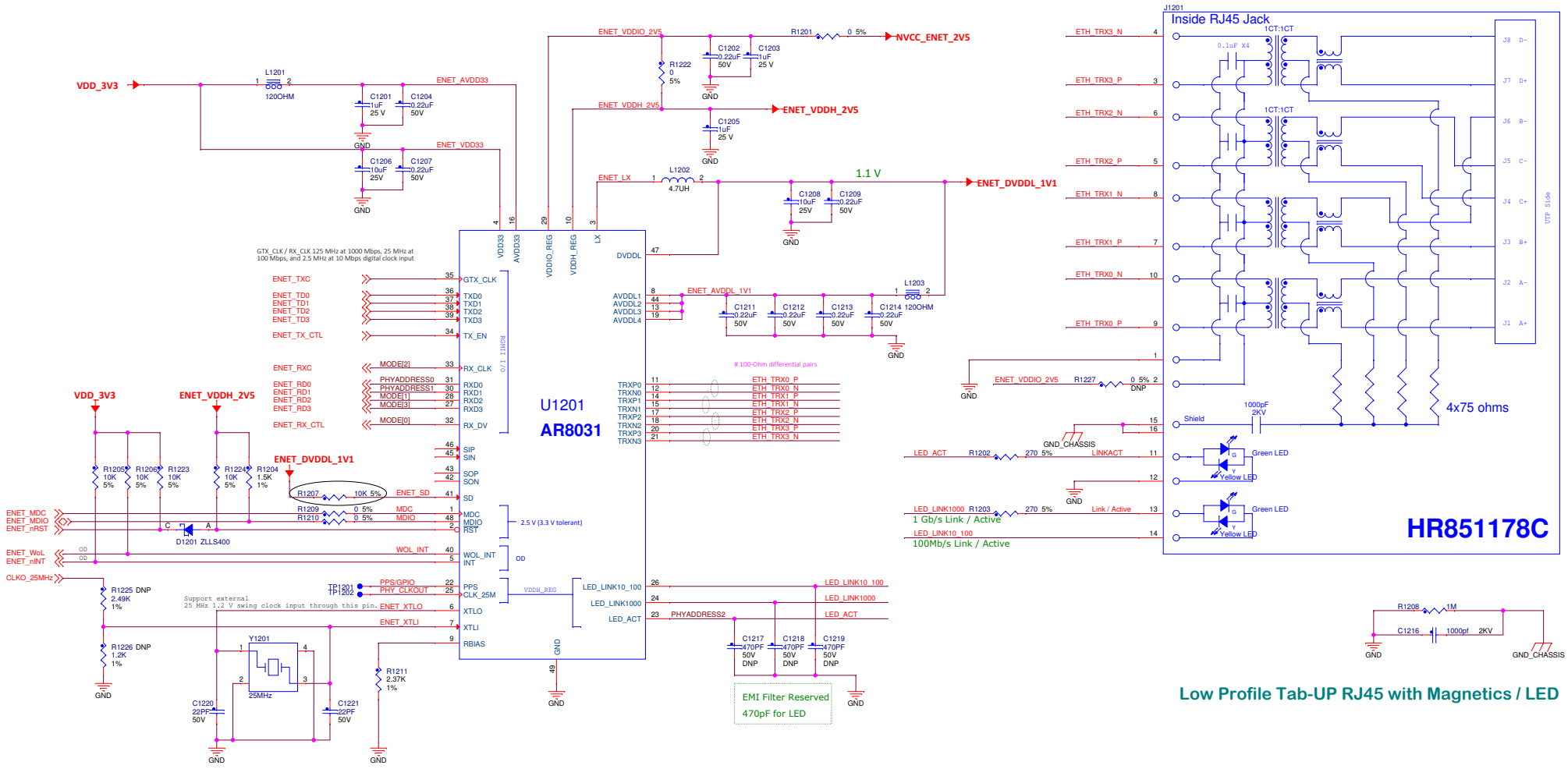


Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: IUO: X PUBI:

Designer: <JW>	Drawing Title: mScale850 EVK		
Drawn by: <JW>	Page Title: CODEC		
Approved: <Approver>	Size C	Document Number SCH-29615 PDF: SPF-29615	Rev B1
	Date: Monday, September 25, 2017	Sheet 14 of 23	

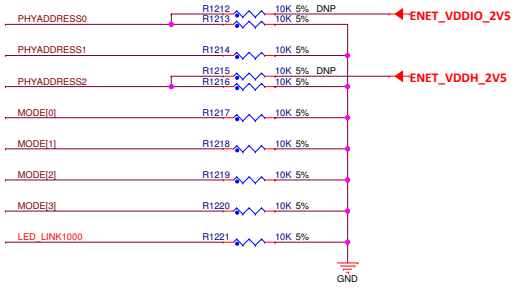
RGMII 10/100/1000 Ethernet

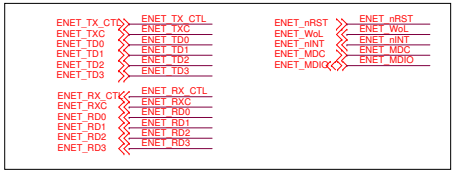


Power-on Strapping Pins

PHY PIN	PHY CFG	Default	Definition
RXD0	PHYADDRESS0	0	LED_ACT and RXD1-0 set the lower three bits of the physical address. The upper two bits of the physical address are set to the default, "00".
RXD1	PHYADDRESS1	0	
LED_ACT	PHYADDRESS2	1	
RX_DV	MODE[0]	0	0000 1000 Base-T, RGMII; 0001 1000 Base-T, SGMII; 0010 1000 Base-X, RGMII, 50Ω; 0011 1000 Base-X, RGMII, 75Ω; 0100 1000 Base-X/T, TRANS, 50Ω; 0101 1000 Base-X/T, TRANS, 75Ω; 0110 100 Base-FX, RGMII, 50Ω; 0111 100 Base-FX/TX, TRANS, 50Ω; 1011 RMII, copper fiber auto-detection; 1110 100 Base-FX, RGMII, 75Ω; 1111 100 Base-FX/TX, TRANS, 75Ω; Others Reserved
RXD2	MODE[1]	0	
RX_CLK	MODE[2]	0	
RXD3	MODE[3]	0	
LED_LINK1000	INT_SELECT	1	0: INT ; 1:GPIO

Power-on Strapping Pins CFG



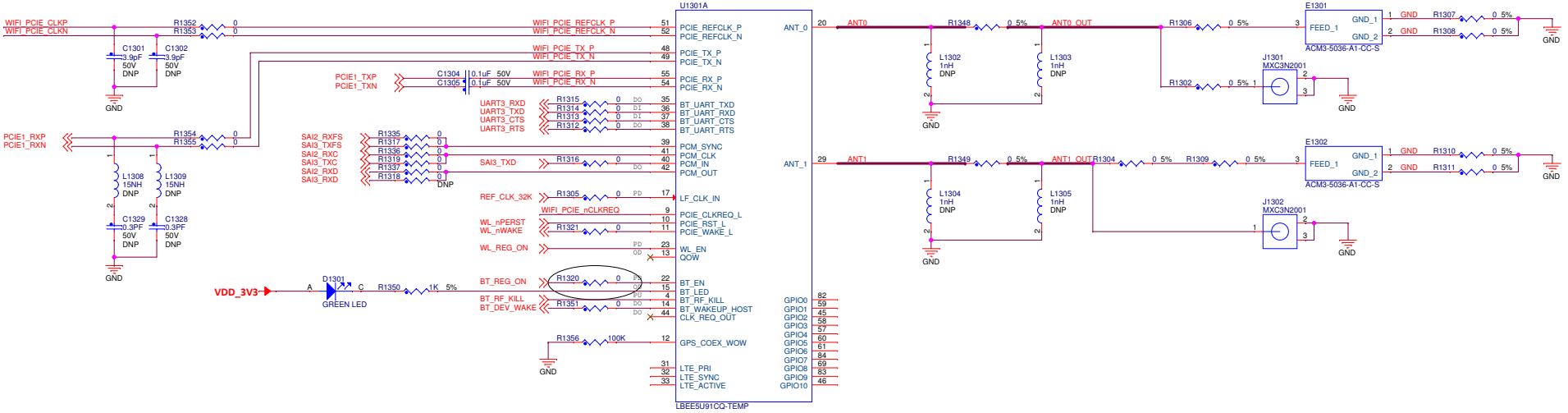


Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: IUO: X PUBI:

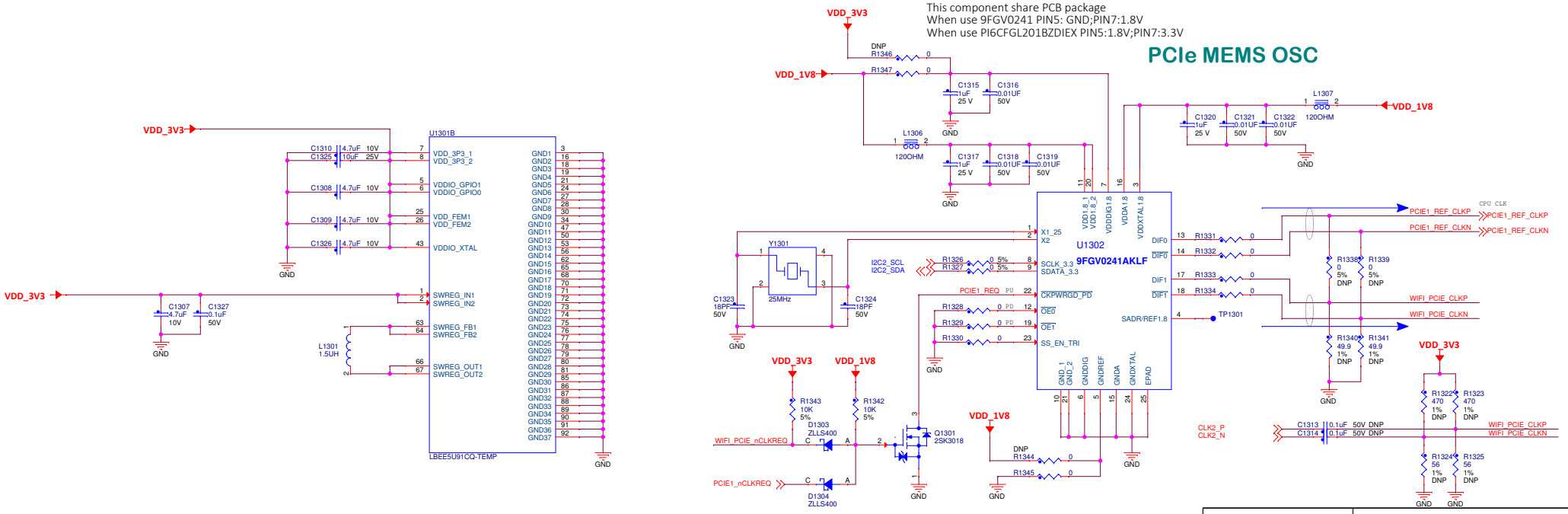
Designer: <JW>	Drawing Title: mScale850 EVK	
Drawn by: <JW>	Page Title: Ethernet	
Approved: <Approver>	Size: C	Document Number: SCH-29615 PDF: SPF-29615 Rev: B1
	Date: Monday, September 25, 2017	Sheet 15 of 23

WiFi/BT 802.11a/b/g/n/ac + Bluetooth 4.1/ EDR



NOTE:
This component share PCB package
When use 9FGV0241 PIN5: GND;PIN7:1.8V
When use PI6CFGL201BZDIEX PIN5:1.8V;PIN7:3.3V

PCIe MEMS OSC



NXP	**Microcontroller Product Group**	
	6501 William Cannon Drive West Austin, TX 78735-8598	

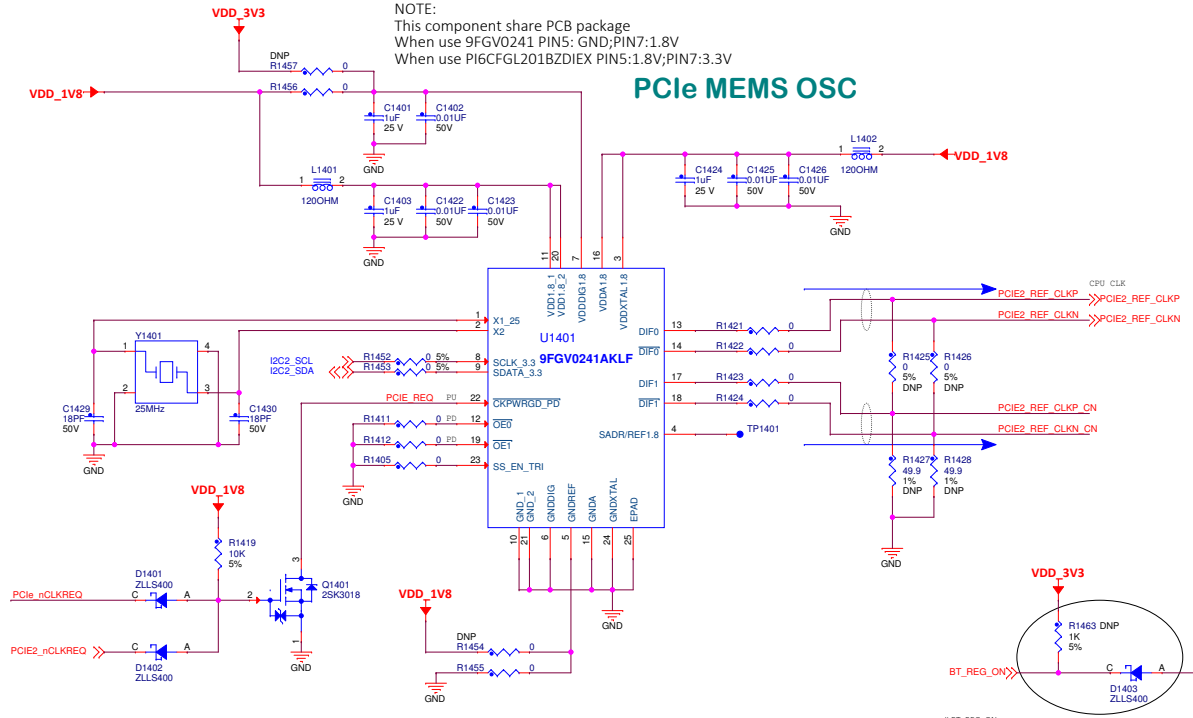
ICAP Classification: CP: IUO: X PUBI:

Designer: <JW>	Drawing Title: **mScale850 EVK**		
Drawn by: <JW>	Page Title: **WiFi/BT**		
Approved: <Approver>	Size: C	Document Number: SCH-29615 PDF: SPF-29615	Rev: B1
	Date: Monday, September 25, 2017	Sheet 16 of 23	

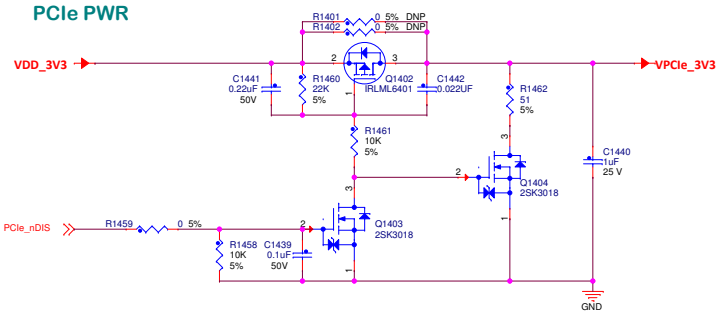
PCIe M.2/NGFF

NOTE:
This component share PCB package
When use 9FGV0241 PIN5: GND;PIN7:1.8V
When use PI6CFGL201BZDIEX PIN5:1.8V;PIN7:3.3V

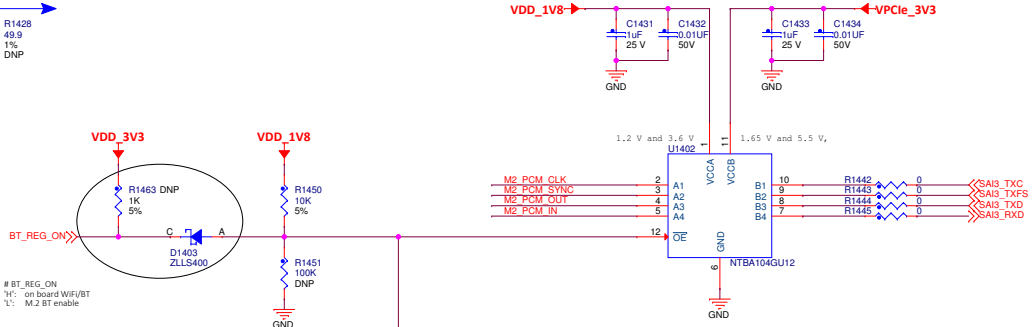
PCIe MEMS OSC



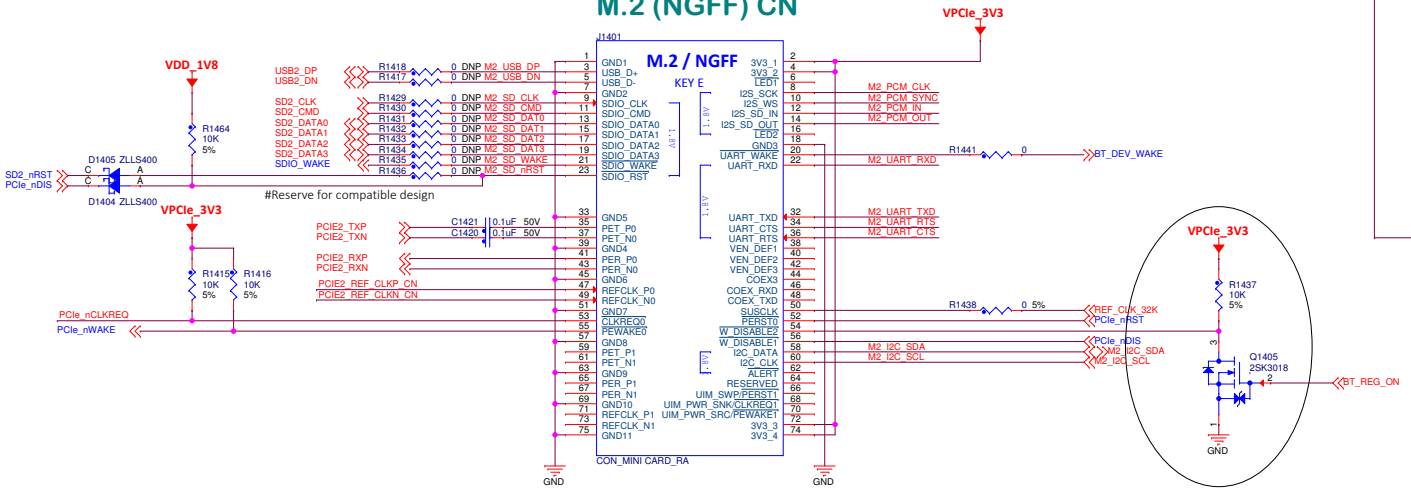
PCIe PWR

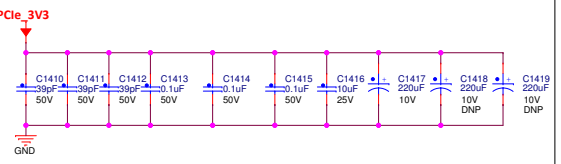


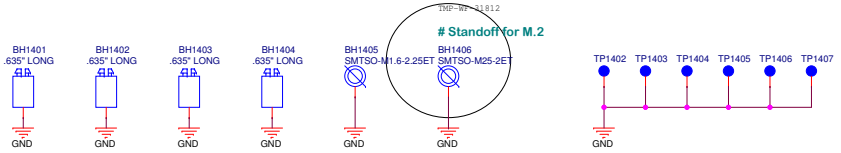
3.3V->1.8V Level Shifter



M.2 (NGFF) CN







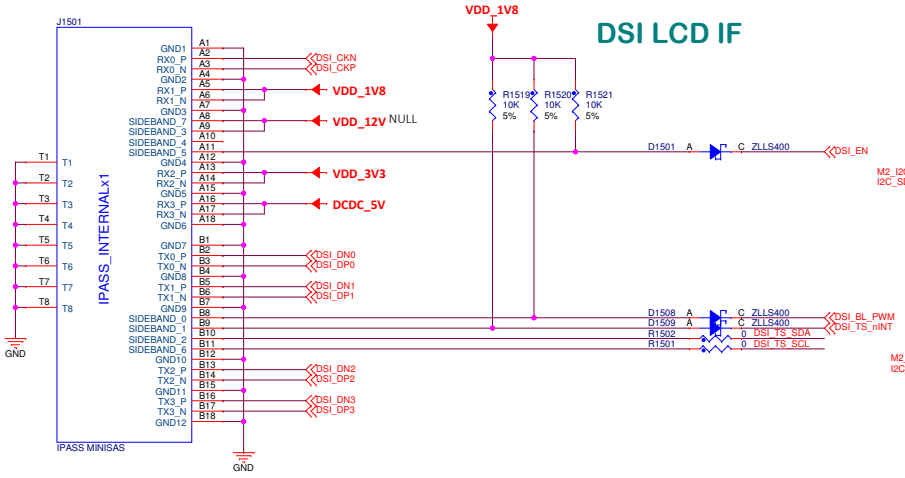
Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: IUO: X PUBI:

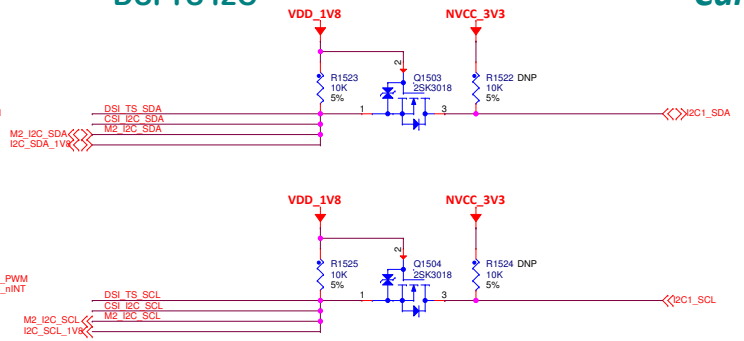
Designer: <JW>	Drawing Title: mScale850 EVK		
Drawn by: <JW>	Page Title: mini-PCIe		
Approved: <Approver>	Size C	Document Number SCH-29615 PDF: SPF-29615	Rev B1
	Date: Tuesday, September 26, 2017	Sheet 17 of 23	

Camera/DSI LCD

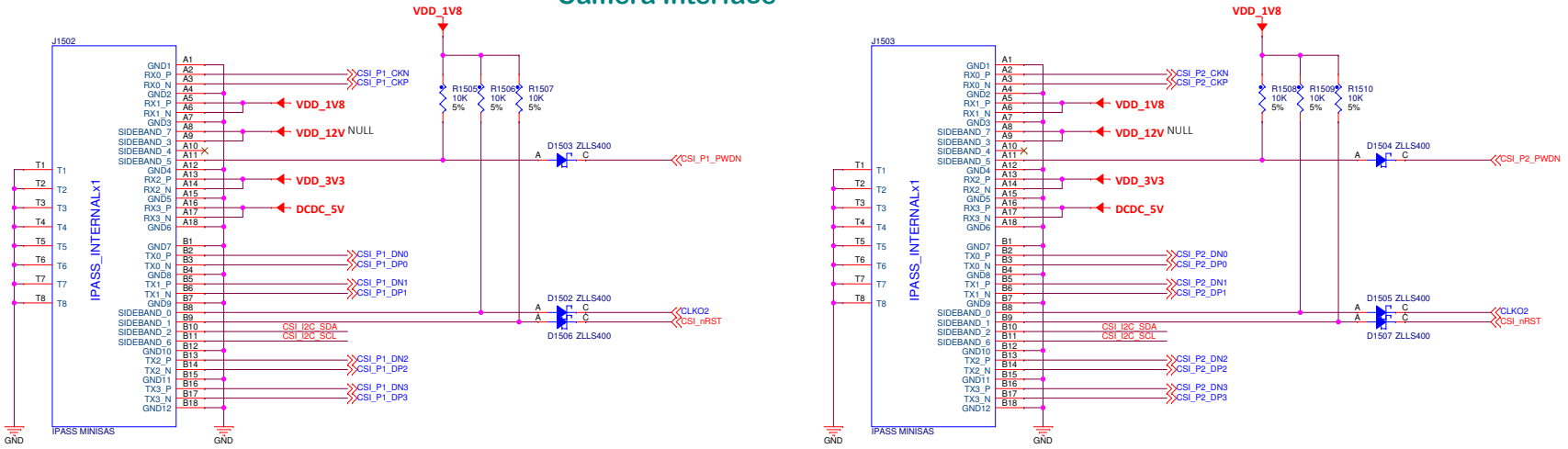
DSI LCD IF

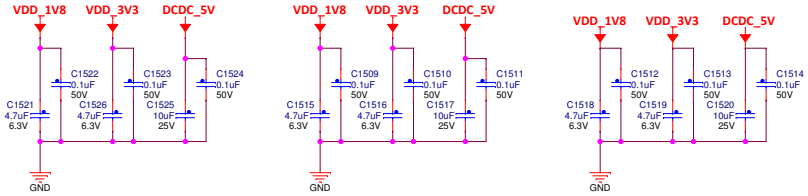


DSI TS I2C



Camera Interface



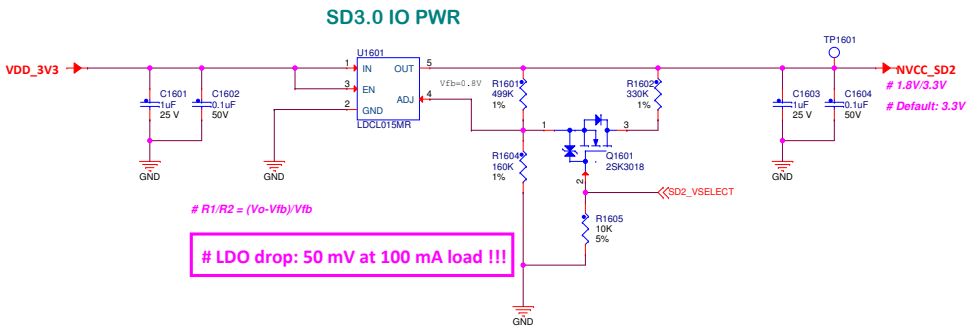


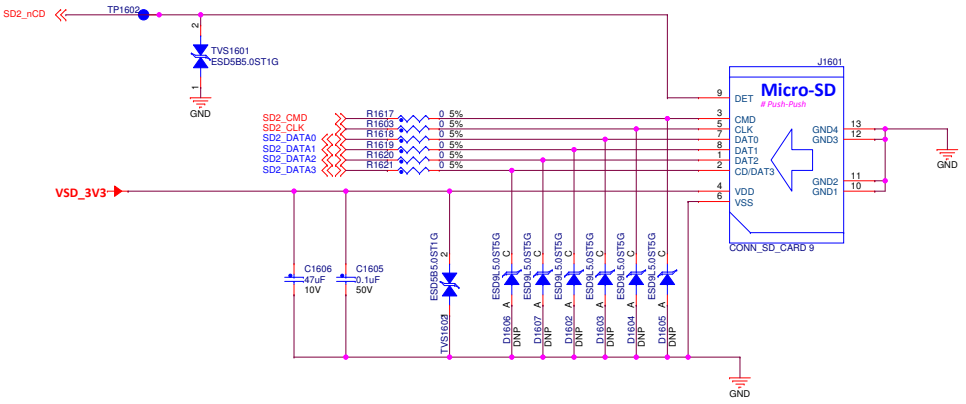
Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

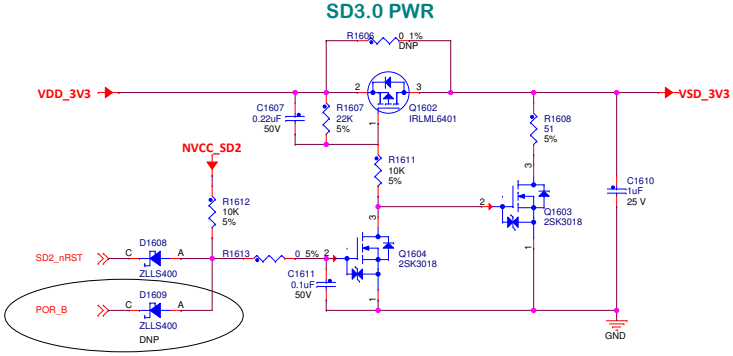
ICAP Classification: CP: IUO: X PUBI:

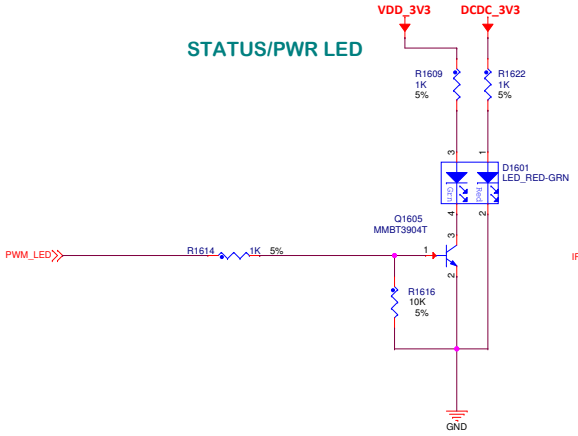
Designer: <JW>	Drawing Title: mScale850 EVK		
Drawn by: <JW>	Page Title: MIPI/DSI/CSI		
Approved: <Approver>	Size C	Document Number SCH-29615 PDF: SPF-29615	Rev B1
	Date: Monday, September 25, 2017	Sheet 18 of 23	

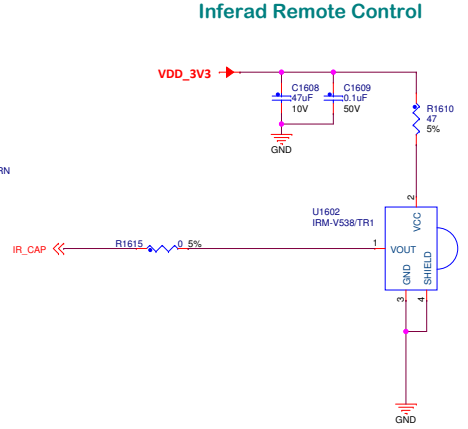
MicroSD/Infrared/LED





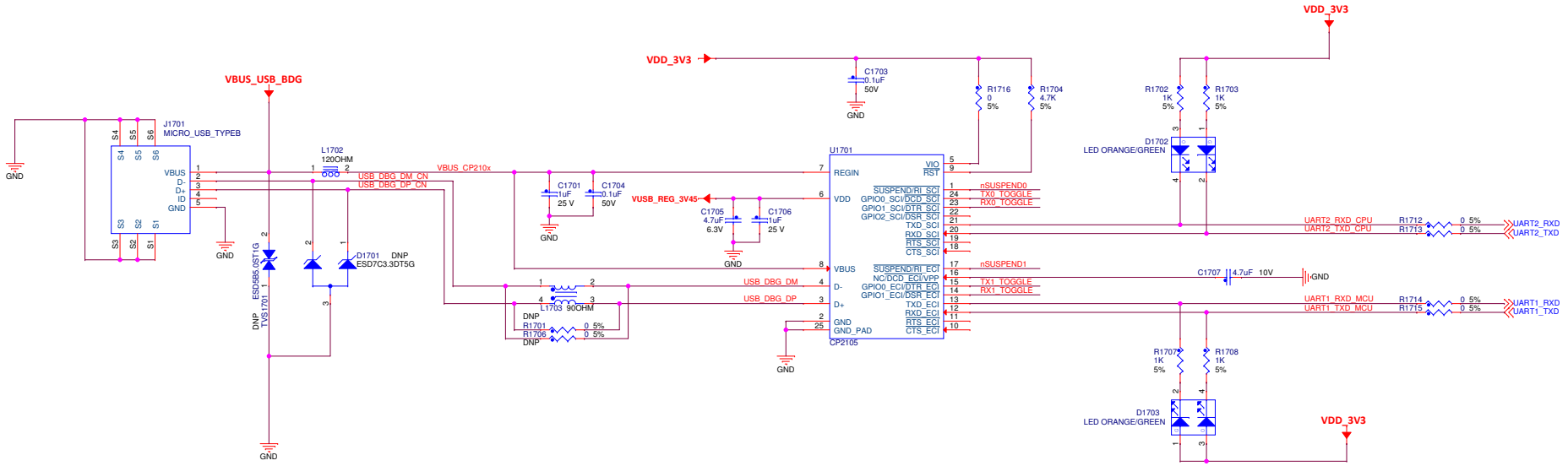




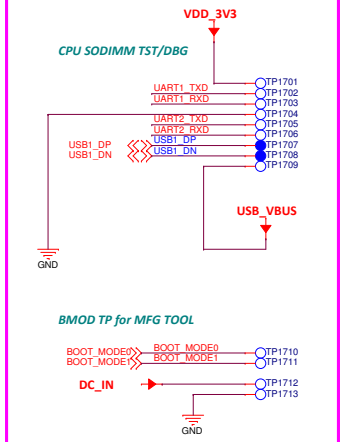


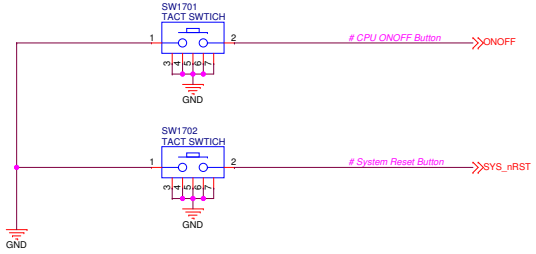
NXP	Microcontroller Product Group 6501 William Cannon Drive West Austin, TX 78735-8598	
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.		
ICAP Classification: CP: IUO: X PUBI:		
Designer: <JW>	Drawing Title: mScale850 EVK	
Drawn by: <JW>	Page Title: SD/IR/LED/BTN	
Approved: <Approver>	Size C / Document Number SCH-29615 PDF: SPF-29615	Rev B1
	Date: Monday, September 25, 2017	Sheet 19 of 23

UART-USB DBG



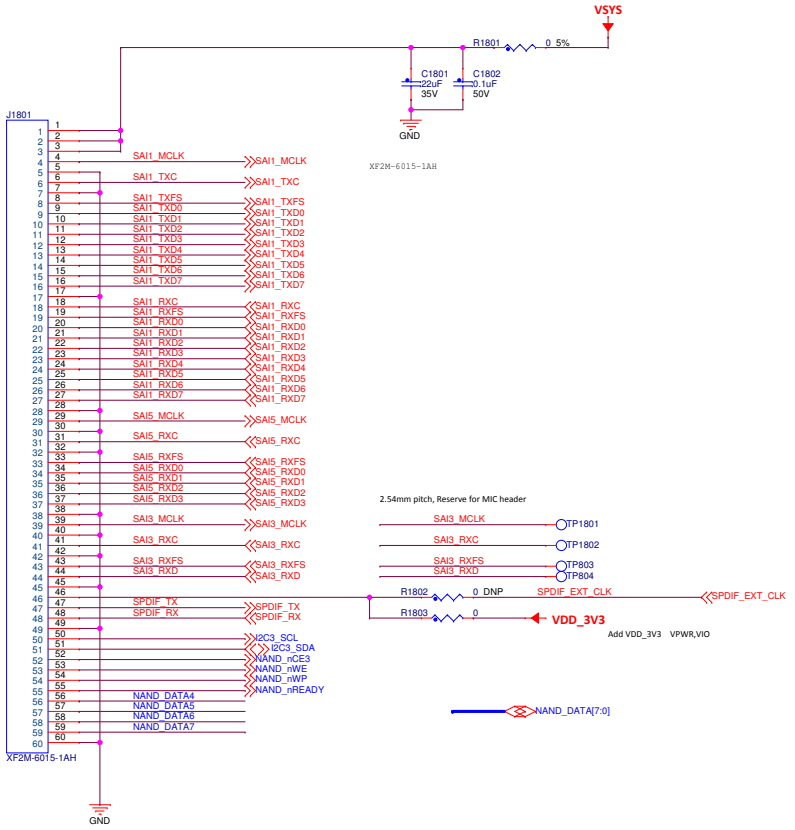
TP for on-line MFG





NXP	Microcontroller Product Group 6501 William Cannon Drive West Austin, TX 78735-8598	
This document contains information proprietary to NXP and shall not be used for engineering design, procurement or manufacture in whole or in part without the express written permission of NXP Semiconductors.		
ICAP Classification: CP: IUO: X PUBI:		
Designer: <JW>	Drawing Title: mScale850 EVK	
Drawn by: <JW>	Page Title: Debug UART	
Approved: <Approver>	Size C / Document Number SCH-29615 PDF: SPF-29615	Rev B1
	Date: Monday, September 25, 2017	Sheet 20 of 23

EXP CN



Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: IUO: X PUBI:

Designer: <JW>	Drawing Title: mScale850 EVK		
Drawn by: <JW>	Page Title: Expansion CN		
Approved: <Approver>	Size C	Document Number SCH-29615 PDF: SPF-29615	Rev B1
	Date: Monday, September 25, 2017	Sheet 21 of 23	

NOTE:

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: IUO: X PUBI:

Designer: <JW>	Drawing Title: mScale850 EVK	
Drawn by: <JW>	Page Title: NOTE	
Approved: <Approver>	Size: C	Document Number: SCH-29615 PDF: SPF-29615 — Rev: B1
	Date: Monday, September 25, 2017	Sheet 22 of 23

i.MX8M IOMUX

NAME	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	Alt6 Special EN	ALT7	Alt7 Special EN
TEST_MODE	tcu.TEST_MODE	tcu.TEST_MODE									
BOOT_MODE0	ccmsrcgpcmix.BOOT_MODE[0]	ccmsrcgpcmix.BOOT_MODE[0]									
BOOT_MODE1	ccmsrcgpcmix.BOOT_MODE[1]	ccmsrcgpcmix.BOOT_MODE[1]									
JTAG_MOD	cjtag_wrapper.MOD	cjtag_wrapper.MOD									
JTAG_TRST_B	cjtag_wrapper.TRST_B	cjtag_wrapper.TRST_B									
JTAG_TDI	cjtag_wrapper.TDI	cjtag_wrapper.TDI									
JTAG_TMS	cjtag_wrapper.TMS	cjtag_wrapper.TMS									
JTAG_TCK	cjtag_wrapper.TCK	cjtag_wrapper.TCK									
JTAG_TDO	cjtag_wrapper.TDO	cjtag_wrapper.TDO									
RTC	snvsmix.RTC	snvsmix.RTC									
PMIC_STBY_REQ	ccmsrcgpcmix.PMIC_STBY_REQ	ccmsrcgpcmix.PMIC_STBY_REQ									
PMIC_ON_REQ	snvsmix.PMIC_ON_REQ	snvsmix.PMIC_ON_REQ									
ONOFF	snvsmix.ONOFF	snvsmix.ONOFF									
POR_B	snvsmix.POR_B	snvsmix.POR_B									
RTC_RESET_B	snvsmix.RTC_POR_B	snvsmix.RTC_RESET_B									
GPIO1_IO00	gpio1.IO[0]	gpio1.IO[0]	ccmsrcgpcmix.ENET_PHY_REF_CLK_ROOT				anamix.REF_CLK_32K	ccmsrcgpcmix.EXT_CLK1		sjc.FAIL	
GPIO1_IO01	gpio1.IO[1]	gpio1.IO[1]	pwm1.OUT				anamix.REF_CLK_24M	ccmsrcgpcmix.EXT_CLK2		sjc.ACTIVE	ccmsrcgpcmix.src_system_rst
GPIO1_IO02	gpio1.IO[2]	gpio1.IO[2]	wdog1.WDOG_B				wdog1.WDOG_ANY			sjc.DE_B	sjc.sjc_gpucr1_reg[30]
GPIO1_IO03	gpio1.IO[3]	gpio1.IO[3]	usdhc1.VSELECT				sdma1.EXT_EVENT[0]	anamix.xtal_ok		sjc.DONE	
GPIO1_IO04	gpio1.IO[4]	gpio1.IO[4]	usdhc2.VSELECT				sdma1.EXT_EVENT[1]	anamix.xtal_ok_lv		usdhc1.TEST_TRIG	
GPIO1_IO05	gpio1.IO[5]	gpio1.IO[5]	m4.NMI				ccmsrcgpcmix.PMIC_READY	ccmsrcgpcmix.INT_BOOT	ccmsrcgpcmix.src_system_rst	usdhc2.TEST_TRIG	
GPIO1_IO06	gpio1.IO[6]	gpio1.IO[6]	enet1.MDC				usdhc1.CD_B	ccmsrcgpcmix.EXT_CLK3		ecspi1.TEST_TRIG	
GPIO1_IO07	gpio1.IO[7]	gpio1.IO[7]	enet1.MDIO				usdhc1.WP	ccmsrcgpcmix.EXT_CLK4		ecspi2.TEST_TRIG	
GPIO1_IO08	gpio1.IO[8]	gpio1.IO[8]	enet1.1588_EVENT0_IN				usdhc2.RESET_B	ccmsrcgpcmix.WAIT		qspi.TEST_TRIG	
GPIO1_IO09	gpio1.IO[9]	gpio1.IO[9]	enet1.1588_EVENT0_OUT				sdma2.EXT_EVENT[0]	ccmsrcgpcmix.STOP		rawnand.TEST_TRIG	
GPIO1_IO10	gpio1.IO[10]	gpio1.IO[10]	usb1.OTG_ID							ocotp_ctrl_wrapper.FUSE_LATCHED	sjc.sjc_gpucr3_reg[14]
GPIO1_IO11	gpio1.IO[11]	gpio1.IO[11]	usb2.OTG_ID				ccmsrcgpcmix.PMIC_READY			caam_wrapper.RNG_OSC_OBS	
GPIO1_IO12	gpio1.IO[12]	gpio1.IO[12]	usb1.OTG_PWR				sdma2.EXT_EVENT[1]	ccmsrcgpcmix.OUT0		csu.CSU_ALARM_AUT[0]	
GPIO1_IO13	gpio1.IO[13]	gpio1.IO[13]	usb1.OTG_OC				pwm2.OUT	ccmsrcgpcmix.OUT1		csu.CSU_ALARM_AUT[1]	
GPIO1_IO14	gpio1.IO[14]	gpio1.IO[14]	usb2.OTG_PWR				pwm3.OUT	ccmsrcgpcmix.OUT2		csu.CSU_ALARM_AUT[2]	
GPIO1_IO15	gpio1.IO[15]	gpio1.IO[15]	usb2.OTG_OC				pwm4.OUT	ccmsrcgpcmix.CLKO1		csu.CSU_INT_DEB	
ENET_MDC	gpio1.IO[16]	enet1.MDC					gpio1.IO[16]	ccmsrcgpcmix.CLKO2			
ENET_MDIO	gpio1.IO[17]	enet1.MDIO					gpio1.IO[17]				
ENET_TD3	gpio1.IO[18]	enet1.RGMII_TD3					gpio1.IO[18]				
ENET_TD2	gpio1.IO[19]	enet1.RGMII_TD2	"INPUT=enet1.TX_CLK				gpio1.IO[19]				
ENET_TD1	gpio1.IO[20]	enet1.RGMII_TD1	OUTPUT=ccmsrcgpcmix.ENET_REF_CLK_ROOT"				gpio1.IO[20]				
ENET_TD0	gpio1.IO[21]	enet1.RGMII_TD0					gpio1.IO[21]				
ENET_TX_CTL	gpio1.IO[22]	enet1.RGMII_TX_CTL					gpio1.IO[22]				
ENET_TXC	gpio1.IO[23]	enet1.RGMII_TXC					gpio1.IO[23]				
ENET_RX_CTL	gpio1.IO[24]	enet1.RGMII_RX_CTL	enet1.TX_ER				gpio1.IO[24]				
ENET_RXC	gpio1.IO[25]	enet1.RGMII_RXC					gpio1.IO[25]				
ENET_RD0	gpio1.IO[26]	enet1.RGMII_RD0	enet1.RX_ER				gpio1.IO[26]				
ENET_RD1	gpio1.IO[27]	enet1.RGMII_RD1					gpio1.IO[27]				
ENET_RD2	gpio1.IO[28]	enet1.RGMII_RD2					gpio1.IO[28]				
ENET_RD3	gpio1.IO[29]	enet1.RGMII_RD3					gpio1.IO[29]				
SD1_CLK	gpio2.IO[0]	usdhc1.CLK					gpio2.IO[0]				
SD1_CMD	gpio2.IO[1]	usdhc1.CMD					gpio2.IO[1]				
SD1_DATA0	gpio2.IO[2]	usdhc1.DATA0					gpio2.IO[2]				
SD1_DATA1	gpio2.IO[3]	usdhc1.DATA1					gpio2.IO[3]				
SD1_DATA2	gpio2.IO[4]	usdhc1.DATA2					gpio2.IO[4]				
SD1_DATA3	gpio2.IO[5]	usdhc1.DATA3					gpio2.IO[5]				
SD1_DATA4	gpio2.IO[6]	usdhc1.DATA4					gpio2.IO[6]				
SD1_DATA5	gpio2.IO[7]	usdhc1.DATA5					gpio2.IO[7]				
SD1_DATA6	gpio2.IO[8]	usdhc1.DATA6					gpio2.IO[8]				
SD1_DATA7	gpio2.IO[9]	usdhc1.DATA7					gpio2.IO[9]				
SD1_RESET_B	gpio2.IO[10]	usdhc1.RESET_B					gpio2.IO[10]				
SD1_STROBE	gpio2.IO[11]	usdhc1.STROBE					gpio2.IO[11]				
SD2_CD_B	gpio2.IO[12]	usdhc2.CD_B					gpio2.IO[12]				
SD2_CLK	gpio2.IO[13]	usdhc2.CLK					gpio2.IO[13]	ccmsrcgpcmix.OBSERVE0		observe_mux.OUT[0]	
SD2_CMD	gpio2.IO[14]	usdhc2.CMD					gpio2.IO[14]	ccmsrcgpcmix.OBSERVE1		observe_mux.OUT[1]	
SD2_DATA0	gpio2.IO[15]	usdhc2.DATA0					gpio2.IO[15]	ccmsrcgpcmix.OBSERVE2		observe_mux.OUT[2]	
SD2_DATA1	gpio2.IO[16]	usdhc2.DATA1					gpio2.IO[16]	ccmsrcgpcmix.WAIT		observe_mux.OUT[3]	
SD2_DATA2	gpio2.IO[17]	usdhc2.DATA2					gpio2.IO[17]	ccmsrcgpcmix.STOP		observe_mux.OUT[4]	
SD2_DATA3	gpio2.IO[18]	usdhc2.DATA3					gpio2.IO[18]	ccmsrcgpcmix.EARLY_RESET	sjc.sjc_gpucr3_reg[14]		
SD2_RESET_B	gpio2.IO[19]	usdhc2.RESET_B					gpio2.IO[19]	ccmsrcgpcmix.SYSTEM_RESET	sjc.sjc_gpucr3_reg[14]		
SD2_WP	gpio2.IO[20]	usdhc2.WP					gpio2.IO[20]				
NAND_ALE	gpio3.IO[0]	rawnand.ALE					gpio3.IO[0]			sim_m.HMASTLOCK	sjc.sjc_gpucr1_reg[11]
NAND_CE0_B	gpio3.IO[1]	rawnand.CE0_B	qspi.A_SCLK				gpio3.IO[1]			sim_m.HPROT[0]	sjc.sjc_gpucr1_reg[11]
NAND_CE1_B	gpio3.IO[2]	rawnand.CE1_B	qspi.A_SS0_B				gpio3.IO[2]			sim_m.HPROT[1]	sjc.sjc_gpucr1_reg[11]
NAND_CE2_B	gpio3.IO[3]	rawnand.CE2_B	qspi.A_SS1_B				gpio3.IO[3]			sim_m.HPROT[2]	sjc.sjc_gpucr1_reg[11]
NAND_CE3_B	gpio3.IO[4]	rawnand.CE3_B	qspi.B_SS0_B				gpio3.IO[4]			sim_m.HPROT[3]	sjc.sjc_gpucr1_reg[11]
NAND_CLE	gpio3.IO[5]	rawnand.CLE	qspi.B_SS1_B				gpio3.IO[5]			sim_m.HADDR[0]	sjc.sjc_gpucr1_reg[11]
NAND_DATA00	gpio3.IO[6]	rawnand.DATA00	qspi.B_SCLK				gpio3.IO[6]			sim_m.HADDR[1]	sjc.sjc_gpucr1_reg[11]
NAND_DATA01	gpio3.IO[7]	rawnand.DATA01	qspi.A_DATA[0]				gpio3.IO[7]			sim_m.HADDR[2]	sjc.sjc_gpucr1_reg[11]
NAND_DATA02	gpio3.IO[8]	rawnand.DATA02	qspi.A_DATA[1]				gpio3.IO[8]			sim_m.HADDR[3]	sjc.sjc_gpucr1_reg[11]
NAND_DATA03	gpio3.IO[9]	rawnand.DATA03	qspi.A_DATA[2]				gpio3.IO[9]			sim_m.HADDR[4]	sjc.sjc_gpucr1_reg[11]
NAND_DATA04	gpio3.IO[10]	rawnand.DATA04	qspi.A_DATA[3]				gpio3.IO[10]			sim_m.HADDR[5]	sjc.sjc_gpucr1_reg[11]
NAND_DATA05	gpio3.IO[11]	rawnand.DATA05	qspi.B_DATA[0]				gpio3.IO[11]			sim_m.HADDR[6]	sjc.sjc_gpucr1_reg[11]
NAND_DATA06	gpio3.IO[12]	rawnand.DATA06	qspi.B_DATA[1]				gpio3.IO[12]			sim_m.HADDR[7]	sjc.sjc_gpucr1_reg[11]
NAND_DATA07	gpio3.IO[13]	rawnand.DATA07	qspi.B_DATA[2]				gpio3.IO[13]			sim_m.HADDR[8]	sjc.sjc_gpucr1_reg[11]
NAND_DQS	gpio3.IO[14]	rawnand.DQS	qspi.B_DATA[3]				gpio3.IO[14]			sim_m.HADDR[9]	sjc.sjc_gpucr1_reg[11]
NAND_RE_B	gpio3.IO[15]	rawnand.RE_B	qspi.A_DQS				gpio3.IO[15]			sim_m.HADDR[10]	sjc.sjc_gpucr1_reg[11]
NAND_READY_B	gpio3.IO[16]	rawnand.READY_B	qspi.B_DQS				gpio3.IO[16]			sim_m.HADDR[11]	sjc.sjc_gpucr1_reg[11]
NAND_WE_B	gpio3.IO[17]	rawnand.WE_B					gpio3.IO[17]			sim_m.HADDR[12]	sjc.sjc_gpucr1_reg[11]
NAND_WP_B	gpio3.IO[18]	rawnand.WP_B					gpio3.IO[18]			sim_m.HADDR[13]	sjc.sjc_gpucr1_reg[11]
SAI5_RXFS	gpio3.IO[19]	sai5.RX_SYNC					gpio3.IO[19]			sim_m.HADDR[14]	sjc.sjc_gpucr1_reg[11]
SAI5_RXC	gpio3.IO[20]	sai5.RX_BCLK	sai1.TX_DATA[0]				gpio3.IO[20]				
SAI5_RXD0	gpio3.IO[21]	sai5.RX_DATA[0]	sai1.TX_DATA[1]	sai1.TX_SYNC	sai5.TX_SYNC		gpio3.IO[21]				
SAI5_RXD1	gpio3.IO[22]	sai5.RX_DATA[1]	sai1.TX_DATA[2]	sai1.TX_SYNC	sai5.TX_BCLK		gpio3.IO[22]				
SAI5_RXD2	gpio3.IO[23]	sai5.RX_DATA[2]	sai1.TX_DATA[3]	sai1.TX_SYNC	sai5.TX_DATA[0]		gpio3.IO[23]				
SAI5_RXD3	gpio3.IO[24]	sai5.RX_DATA[3]	sai1.TX_DATA[4]	sai1.TX_SYNC			gpio3.IO[24]				
SAI5_MCLK	gpio3.IO[25]	sai5.MCLK	sai1.TX_DATA[5]	sai4.MCLK			gpio3.IO[25]	ccmsrcgpcmix.TESTER_ACK	~ccmsrcgpcmix.src_en_system_clk		
SAI1_RXFS	gpio4.IO[0]	sai1.RX_SYNC	sai1.TX_BCLK			coresight.TRACE_CLK	gpio4.IO[0]			sim_m.HADDR[15]	sjc.sjc_gpucr1_reg[11]
SAI1_RXC	gpio4.IO[1]	sai1.RX_BCLK	sai5.RX_SYNC			coresight.TRACE_CTL	gpio4.IO[1]			sim_m.HADDR[16]	sjc.sjc_gpucr1_reg[11]
SAI1_RXD0	gpio4.IO[2]	sai1.RX_DATA[0]	sai5.RX_BCLK			coresight.TRACE[0]	gpio4.IO[2]	ccmsrcgpcmix.BOOT_CFG[0]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[17]	sjc.sjc_gpucr1_reg[11]
SAI1_RXD1	gpio4.IO[3]	sai1.RX_DATA[1]	sai5.RX_DATA[0]			coresight.TRACE[1]	gpio4.IO[3]	ccmsrcgpcmix.BOOT_CFG[1]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[18]	sjc.sjc_gpucr1_reg[11]
SAI1_RXD2	gpio4.IO[4]	sai1.RX_DATA[2]	sai5.RX_DATA[1]			coresight.TRACE[2]	gpio4.IO[4]	ccmsrcgpcmix.BOOT_CFG[2]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[19]	sjc.sjc_gpucr1_reg[11]
SAI1_RXD3	gpio4.IO[5]	sai1.RX_DATA[3]	sai5.RX_DATA[2]			coresight.TRACE[3]	gpio4.IO[5]	ccmsrcgpcmix.BOOT_CFG[3]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[20]	sjc.sjc_gpucr1_reg[11]
SAI1_RXD4	gpio4.IO[6]	sai1.RX_DATA[4]	sai5.RX_DATA[3]	sai6.RX_BCLK		coresight.TRACE[4]	gpio4.IO[6]	ccmsrcgpcmix.BOOT_CFG[4]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[21]	sjc.sjc_gpucr1_reg[11]
SAI1_RXD5	gpio4.IO[7]	sai1.RX_DATA[5]	sai6.TX_BCLK	sai6.RX_DATA[0]	sai1.RX_SYNC	coresight.TRACE[5]	gpio4.IO[7]	ccmsrcgpcmix.BOOT_CFG[5]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[22]	sjc.sjc_gpucr1_reg[11]
SAI1_RXD6	gpio4.IO[8]	sai1.RX_DATA[6]	sai6.TX_DATA[0]	sai6.RX_SYNC		coresight.TRACE[6]	gpio4.IO[8]	ccmsrcgpcmix.BOOT_CFG[6]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[23]	sjc.sjc_gpucr1_reg[11]
SAI1_RXD7	gpio4.IO[9]	sai1.RX_DATA[7]	sai6.TX_SYNC	sai1.TX_SYNC	sai1.TX_DATA[4]	coresight.TRACE[7]	gpio4.IO[9]	ccmsrcgpcmix.BOOT_CFG[7]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[24]	sjc.sjc_gpucr1_reg[11]
SAI1_TXFS	gpio4.IO[10]	sai1.TX_SYNC	sai6.MCLK			coresight.EVENTO	gpio4.IO[10]			sim_m.HADDR[25]	sjc.sjc_gpucr1_reg[11]
SAI1_TXC	gpio4.IO[11]	sai1.TX_BCLK	sai5.TX_SYNC			coresight.EVENTI	gpio4.IO[11]			sim_m.HADDR[26]	sjc.sjc_gpucr1_reg[11]
SAI1_TXD0	gpio4.IO[12]	sai1.TX_DATA[0]	sai5.TX_BCLK			coresight.TRACE[8]	gpio4.IO[12]	ccmsrcgpcmix.BOOT_CFG[8]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[27]	sjc.sjc_gpucr1_reg[11]
SAI1_TXD1	gpio4.IO[13]	sai1.TX_DATA[1]	sai5.TX_DATA[0]			coresight.TRACE[9]	gpio4.IO[13]	ccmsrcgpcmix.BOOT_CFG[9]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[28]	sjc.sjc_gpucr1_reg[11]
SAI1_TXD2	gpio4.IO[14]	sai1.TX_DATA[2]	sai5.TX_DATA[1]			coresight.TRACE[10]	gpio4.IO[14]	ccmsrcgpcmix.BOOT_CFG[10]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[29]	sjc.sjc_gpucr1_reg[11]
SAI1_TXD3	gpio4.IO[15]	sai1.TX_DATA[3]	sai5.TX_DATA[2]			coresight.TRACE[11]	gpio4.IO[15]	ccmsrcgpcmix.BOOT_CFG[11]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[30]	sjc.sjc_gpucr1_reg[11]
SAI1_TXD4	gpio4.IO[16]	sai1.TX_DATA[4]	sai5.TX_DATA[3]	sai6.TX_BCLK		coresight.TRACE[12]	gpio4.IO[16]	ccmsrcgpcmix.BOOT_CFG[12]	ccmsrcgpcmix.src_system_rst	sim_m.HADDR[31]	sjc.sjc_gpucr1_reg[11]
SAI1_TXD5	gpio4.IO[17]	sai1.TX_DATA[5]	sai6.RX_BCLK	sai6.TX_DATA[0]		coresight.TRACE[13]	gpio4.IO[17]	ccmsrcgpcmix.BOOT_CFG[13]	ccmsrcgpcmix.src_system_rst	sim_m.HBURST[0]	sjc.sjc_gpucr1_reg[11]
SAI1_TXD6	gpio4.IO[18]	sai1.TX_DATA[6]	sai6.RX_DATA[0]	sai6.TX_SYNC		coresight.TRACE[14]	gpio4.IO[18]	ccmsrcgpcmix.BOOT_CFG[14]	ccmsrcgpcmix.src_system_rst	sim_m.HBURST[1]	sjc.sjc_gpucr1_reg[11]
SAI1_TXD7	gpio4.IO[19]	sai1.TX_DATA[7]	sai6.RX_SYNC			coresight.TRACE[15]	gpio4.IO[19]	ccmsrcgpcmix.BOOT_CFG[15]	ccmsrcgpcmix.src_system_rst	sim_m.HBURST[2]	sjc.sjc_gpucr1_reg[11]
SAI1_MCLK	gpio4.IO[20]	sai1.MCLK	sai6.MCLK		sai1.TX_BCLK		gpio4.IO[20]			sim_m.HRESP	sjc.sjc_gpucr1_reg[11]
SAI2_RXFS	gpio4.IO[21]	sai2.RX_SYNC	sai5.MCLK				gpio4.IO[21]			sim_m.HSIZE[0]	sjc.sjc_gpucr1_reg[11]
SAI2_RXC	gpio4.IO[22]	sai2.RX_BCLK	sai5.TX_SYNC				gpio4.IO[22]			sim_m.HSIZE[1]	sjc.sjc_gpucr1_reg[11]
SAI2_RXD0	gpio4.IO[23]	sai2.RX_DATA[0]	sai5.TX_BCLK				gpio4.IO[23]			sim_m.HSIZE[2]	sjc.sjc_gpucr1_reg[11]
SAI2_TXFS	gpio4.IO[24]	sai2.TX_SYNC	sai5.TX_DATA[0]				gpio4.IO[24]			sim_m.HWRITE	sjc.sjc_gpucr1_reg[11]
SAI2_TXC	gpio4.IO[25]	sai2.TX_BCLK	sai5.TX_DATA[1]				gpio4.IO[25]			sim_m.HREADYOUT	sjc.sjc_gpucr1_reg[11]
SAI2_TXD0	gpio4.IO[26]	sai2.TX_DATA[0]	sai5.TX_DATA[2]				gpio4.IO[26]			tpsmp.CLK	sjc.sjc_gpucr1_reg[11]
SAI2_MCLK	gpio4.IO[27]	sai2.MCLK	sai5.TX_DATA[3]				gpio4.IO[27]			tpsmp.HDATA_DIR	sjc.sjc_gpucr1_reg[11]
SAI3_RXFS	gpio4.IO[28]	sai3.RX_SYNC	sai5.MCLK	sai5.RX_SYNC			gpio4.IO[28]			tpsmp.HTRANS[0]	sjc.sjc_gpucr1_reg[11]
SAI3_RXC	gpio4.IO[29]	sai3.RX_BCLK	gpt1.CAPTURE1	sai5.RX_BCLK			gpio4.IO[29]			tpsmp.HTRANS[1]	sjc.sjc_gpucr1_reg[11]
SAI3_RXD	gpio4.IO[30]	sai3.RX_DATA[0]	gpt1.CAPTURE2	sai5.RX_DATA[0]			gpio4.IO[30]			tpsmp.HDATA[0]	sjc.sjc_gpucr1_reg[11]
SAI3_TXFS	gpio4.IO[31]	sai3.TX_SYNC	gpt1.COMPARE1	sai5.RX_DATA[1]			gpio4.IO[31]			tpsmp.HDATA[1]	sjc.sjc_gpucr1_reg[11]
SAI3_TXC	gpio5.IO[0]	sai3.TX_BCLK	gpt1.CLK	sai5.RX_DATA[2]			gpio5.IO[0]			tpsmp.HDATA[2]	sjc.sjc_gpucr1_reg[11]
SAI3_TXD	gpio5.IO[1]	sai3.TX_DATA[0]	gpt1.COMPARE2	sai5.RX_DATA[3]			gpio5.IO[1]			tpsmp.HDATA[3]	sjc.sjc_gpucr1_reg[11]
SAI3_MCLK	gpio5.IO[2]	sai3.MCLK	gpt1.COMPARE3	sai5.MCLK			gpio5.IO[2]			tpsmp.HDATA[4]	sjc.sjc_gpucr1_reg[11]
SPDIF_TX	gpio5.IO[3]	spdif1.OUT	pwm4.OUT				gpio5.IO[3]			tpsmp.HDATA[5]	sjc.sjc_gpucr1_reg[11]
SPDIF_RX	gpio5.IO[4]	spdif1.IN	pwm3.OUT				gpio5.IO[4]			tpsmp.HDATA[6]	sjc.sjc_gpucr1_reg[11]
SPDIF_EXT_CLK	gpio5.IO[5]	spdif1.EXT_CLK	pwm2.OUT				gpio5.IO[5]			tpsmp.HDATA[7]	sjc.sjc_gpucr1_reg[11]
ECSPI1_SCLK	gpio5.IO[6]	ecspi1.SCLK	pwm1.OUT				gpio5.IO[6]			tpsmp.HDATA[8]	sjc.sjc_gpucr1_reg[11]
ECSPI1_MOSI	gpio5.IO[7]	ecspi1.MOSI	uart3.RX				gpio5.IO[7]			tpsmp.HDATA[9]	sjc.sjc_gpucr1_reg[11]
ECSPI1_MISO	gpio5.IO[8]	ecspi1.MISO	uart3.TX				gpio5.IO[8]			tpsmp.HDATA[10]	sjc.sjc_gpucr1_reg[11]
ECSPI1_SS0	gpio5.IO[9]	ecspi1.SS0	uart3.CTS_B				gpio5.IO[9]			tpsmp.HDATA[11]	sjc.sjc_gpucr1_reg[11]
ECSPI2_SCLK	gpio5.IO[10]	ecspi2.SCLK	uart3.RTS_B				gpio5.IO[10]			tpsmp.HDATA[12]	sjc.sjc_gpucr1_reg[11]
ECSPI2_MOSI	gpio5.IO[11]	ecspi2.MOSI	uart4.RX				gpio5.IO[11]			tpsmp.HDATA[13]	sjc.sjc_gpucr1_reg[11]
ECSPI2_MISO	gpio5.IO[12]	ecspi2.MISO	uart4.TX				gpio5.IO[12]			tpsmp.HDATA[14]	sjc.sjc_gpucr1_reg[11]
ECSPI2_SS0	gpio5.IO[13]	ecspi2.SS0	uart4.CTS_B				gpio5.IO[13]			tpsmp.HDATA[15]	sjc.sjc_gpucr1_reg[11]
I2C1_SCL	gpio5.IO[14]	i2c1.SCL	uart4.RTS_B				gpio5.IO[14]			tpsmp.HDATA[16]	sjc.sjc_gpucr1_reg[11]
I2C1_SDA	gpio5.IO[15]	i2c1.SDA	enet1.MDC				gpio5.IO[15]			tpsmp.HDATA[17]	sjc.sjc_gpucr1_reg[11]
I2C2_SCL	gpio5.IO[16]	i2c2.SCL	enet1.MDIO				gpio5.IO[16]			tpsmp.HDATA[18]	sjc.sjc_gpucr1_reg[11]
I2C2_SDA	gpio5.IO[17]	i2c2.SDA	enet1.1588_EVENT1_IN				gpio5.IO[17]			tpsmp.HDATA[19]	sjc.sjc_gpucr1_reg[11]
I2C3_SCL	gpio5.IO[18]	i2c3.SCL	enet1.1588_EVENT1_OUT	gpt2.CLK			gpio5.IO[18]			tpsmp.HDATA[20]	sjc.sjc_gpucr1_reg[11]
I2C3_SDA	gpio5.IO[19]	i2c3.SDA	pwm4.OUT	gpt3.CLK			gpio5.IO[19]			tpsmp.HDATA[21]	sjc.sjc_gpucr1_reg[11]
I2C4_SCL	gpio5.IO[20]	i2c4.SCL	pwm3.OUT	pcie1.CLKREQ_B			gpio5.IO[20]			tpsmp.HDATA[22]	sjc.sjc_gpucr1_reg[11]
I2C4_SDA	gpio5.IO[21]	i2c4.SDA	pwm2.OUT	pcie2.CLKREQ_B			gpio5.IO[21]			tpsmp.HDATA[23]	sjc.sjc_gpucr1_reg[11]
UART1_RXD	gpio5.IO[22]	uart1.RX	pwm1.OUT				gpio5.IO[22]			tpsmp.HDATA[24]	sjc.sjc_gpucr1_reg[11]
UART1_TXD	gpio5.IO[23]	uart1.TX	ecspi3.SCLK				gpio5.IO[23]			tpsmp.HDATA[25]	sjc.sjc_gpucr1_reg[11]
UART2_RXD	gpio5.IO[24]	uart2.RX	ecspi3.MOSI				gpio5.IO[24]			tpsmp.HDATA[26]	sjc.sjc_gpucr1_reg[11]
UART2_TXD	gpio5.IO[25]	uart2.TX	ecspi3.MISO				gpio5.IO[25]			tpsmp.HDATA[27]	sjc.sjc_gpucr1_reg[11]
UART3_RXD	gpio5.IO[26]	uart3.RX	ecspi3.SS0				gpio5.IO[26]			tpsmp.HDATA[28]	sjc.sjc_gpucr1_reg[11]
UART3_TXD	gpio5.IO[27]	uart3.TX	uart1.CTS_B				gpio5.IO[27]			tpsmp.HDATA[29]	sjc.sjc_gpucr1_reg[11]
UART4_RXD	gpio5.IO[28]	uart4.RX	uart1.RTS_B	pcie1.CLKREQ_B			gpio5.IO[28]			tpsmp.HDATA[30]	sjc.sjc_gpucr1_reg[11]
UART4_TXD	gpio5.IO[29]	uart4.TX	uart2.CTS_B	pcie2.CLKREQ_B			gpio5.IO[29]			tpsmp.HDATA[31]	sjc.sjc_gpucr1_reg[11]
			uart2.RTS_B								

PIN LIST 2.0

Microcontroller Product Group
6501 William Cannon Drive West
Austin, TX 78735-8598

ICAP Classification: CP: IUO: X PUBI:

Designer: <JW>	Drawing Title: mScale850 EVK	
Drawn by: <JW>	Page Title: IOMUX	
Approved: <Approver>	Size: Custom	Document Number: SCH-29615 PDF: SPF-29615 Rev: B1
	Date: Monday, September 25, 2017	Sheet 23 of 23